The Pennsylvania State University

The Graduate School

Department of Computer Engineering

Design of an Upgraded Electronics Control System for An Advanced Lidar Atmospheric Profiling System

A Thesis in
Computer Engineering

by
Alexander D. Achey

Submitted in Partial Fulfillment
of the Requirements
for the Degree of

Master of Science

May 2002

We approve the thesis of Alexander D. Achey.

Date of Signature

_____ _____

C. Russell Philbrick
Professor of Electrical Engineering
Thesis Advisor

_____ _____

Lee D. Coraor
Associate Professor of Computer Science and Engineering
Thesis Advisor

_____ _____

Vijaykrishnan Narayanan
Assistant Professor of Computer Science and Engineering

Abstract

The PSU Lidar Atmospheric Profile Sensor (LAPS) instrument has been used to measure a variety of atmospheric properties including water vapor, temperature, optical extinction and ozone since its design and construction in 1995. Originally designed for the US Navy as an ADM (Advanced Development Model) prototype, the system has since changed its role to a more research oriented tool after being used to demonstrate its ability to meet the required performance goals. It is currently being used as a test-bed for concepts to be integrated into the next generation Advanced LAPS (ALAPS) unit which will be the EDM (Engineering Design Model) used to demonstrate the fit form and function prior to commercial development. Changes in the intended usage of the system, as well as various shortcomings noted in the original design during the six years of its operation, have motivated the need for a redesign of the control computer system for the unit. This update was seen as a first step in moving towards the ALAPS system. In order to meet the new requirements as a research tool, a system with a great deal of flexibility was desired while increasing reliability over the current version. The original system was based on the aging and essentially outdated STD bus standard which is being phased out, hence the more current PC/104 standard has been used to allow future addition of new peripheral devices. Another significant goal was to use the largest possible amount of Commercial Off The Shelf technology (COTS) hardware possible since this will ease repair of the unit, reduce costs, and ease its eventual transition to a manufactured system.

In addition to these main goals, advances in the computer industry as well as reductions in electronics size have led to the possibility of moving portions of the

electronics which currently reside outside the system into the interior of the unit. This redistribution of system electronics will shift a large part of the computing requirements from the external console computer to the internal deck computer. This computer must be able to handle the new data processing and information serving roles while maintaining a fast response to time-critical systems For these reasons, the RT-Linux operating system was chosen to drive the new computer system since it allows for remote access, file serving, hard real-time performance as well as providing good stability with a minimum amount of overhead. Digital and analog signal conditioning modules are also used to provide both electrical isolation and flexibility in the new system.

Table of Contents

List Of Figures

List Of Tables

Acknowledgments

To be completed later…

Chapter 1: Introduction

The Penn State Lidar Atmospheric Profiling System, or LAPS, is the most recent in a series of five lidar systems designed and developed to advance lidar technology during the past 25 years. Development of the LAPS has been supported by the US Navy in an attempt to accurately measure vertical profiles of the temperature and water vapor concentration in the lower atmosphere. The temperature and water vapor data can then be combined to produce profiles of RF refractivity for analysis of RF propagation[10]. Optical extinction measurements are also obtained which provide a real-time measurement of visibility. The LAPS unit was designed and built in the 1994 to 1995 timeframe as an ADM (Advanced Development Model) prototype for an EDM (Engineering Design Model) instrument which would be referred to as the Advanced Lidar Atmospheric Profiling System, or ALAPS. The ALAPS system is meant to be the final prototype for a production system that could be used on naval vessels. For the ALAPS system, the primary design goals from the Navy relevant to this thesis are as follows[10]:

- Move the counting electronics and detector box into the deck unit to yield a closed system and provide processed data as an output with raw counts available on request
- Reduce the size of the deck unit, including the incorporated new electronics and detector, into a volume of approximately one cubic meter
- Increase the profile resolution from the current 75 meters to better than 15 meters

- Operate using the 3rd harmonic of the laser (355 nm) to provide improved signal and data range over the 4th harmonic (266nm) while still remaining in the eye-safe UV region of the spectrum
- To the largest possible degree, use Commercial Off The Shelf (COTS) components in order to ease repair and lower production complications

Since 1996, the LAPS unit has also been used for studying ozone concentrations in the atmosphere for investigations of air quality. For this reason, the LAPS system must retain its current functionality, particularly the 4th harmonic capabilities which allow ozone measurements, while verifying the feasibility of concepts to be included in ALAPS. The upgrades covered in this thesis will be discussed as a means of working towards these goals while also providing the existing LAPS unit with the flexibility it needs to perform its present function as a research instrument and concept test-bed instead of its previous role as a prototype. This will involve the use of a hard real-time operating system, specifically RT-Linux, on an embedded computer as well as interfaces to a variety of signal conditioning modules and legacy hardware. A thorough explanation and description of the existing system will also be provided as a reference as much of the work involved in this thesis came from assembling a coherent picture of the system operation. This was necessary as the overall picture of the system electronics has fluctuated from its initial designs. Next, the strategy for transitioning from the existing system to the new system will be presented. After this, the details of the system's implementation will be given followed by a summary of observed performances and a suggested progression from this foundation to the ALAPS system.

Chapter 2: Existing LAPS Design and ALAPS Goals

In this section, an overview of the LAPS system, as it existed in the Fall of 2001 before the work on the deck computer took place, will be given with emphasis on the electronics and computer control. Information will also be provided throughout on some of the established goals for ALAPS which relate to these subsystems. This information is provided as a background on which many of the design decisions will be based, as well as providing a known previous state to assist in debugging problems that may arise in testing the redesigned system. An overview of the basic elements of the system design significant for this thesis is summarized below in Figure 2.1. The major subsystems of LAPS are separated in to two pieces of equipment, the Console and the Deck units. For the ALAPS system, the counting electronics and detector box will be moved into the deck unit leaving only a network connection to an external control computer for the Console. A more detailed interconnection block diagram is given in Figure 2.2. Note that some of the items shown in Figure 2.2 will not be referred to heavily in this thesis but are included for sake of completeness. In addition, note that Figure 2.2 shows only logic and control connections while omitting power, high voltage and other such connections.

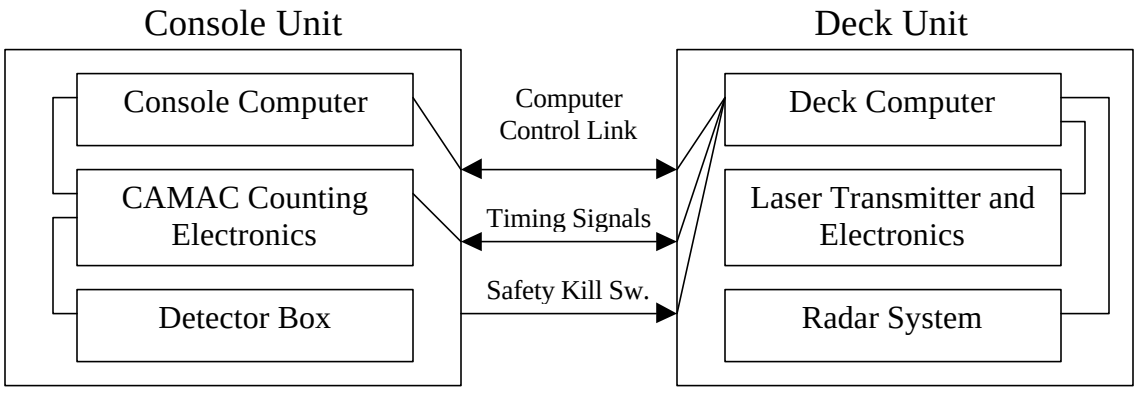


Figure 2.1: LAPS Overview

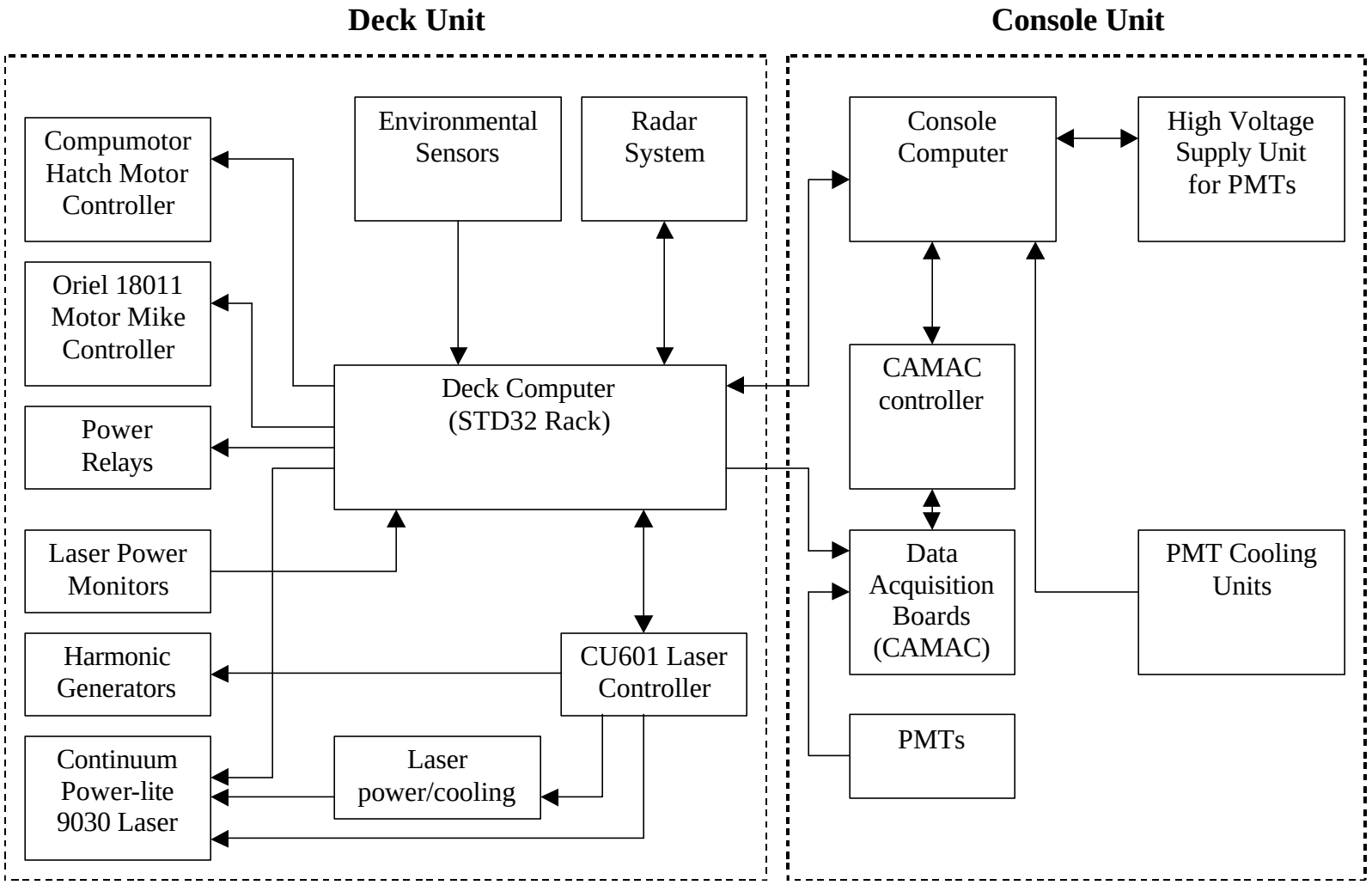


Figure 2.2: LAPS System Control Interconnection Detail

2.1 LAPS Console Unit

In designing the original LAPS system, the Console unit was intended to be the portion of the system which would reside inside the ship. The original Console contained two computers, both running Windows 3.11. The "Data Display" computer was used to display the real-time data product while the "LAPS Command" computer was used both to control the system via the RS-232 link to the deck computer and acquire data from the CAMAC counting electronics. The two were combined into one computer running Windows 2000 over the spring of 2001 due to the availability of faster computers with improved multitasking capabilities and because of frequent problems in communication between the Display and Command computers. Some general information concerning this change is given in Appendix C.

The console also houses the optical detector box containing the photo-multiplier tubes (PMTs) and optics for photon counting return signals at the necessary wavelengths. One of the goals of ALAPS is to transfer both the detector box and photon counting subsystems into the deck unit leaving only an external "Console" computer to control instrument operation and display results. This new computer would have no special hardware and could be a standard portable (laptop) computer, though it will likely be a multi-monitor computer system for displaying data products.

The detector box unit is currently one of the primary areas in which the system needs to be heavily modified in order to meet the ALAPS design goals; however, plans are well underway towards the new design. These plans should reduce the detector box size to the point where it will fit into a standard 19" rack, occupying approximately 12" of vertical space for the self-calibrating design[7]. These new plans include a new PMT

front end based on the R7400 series from Hamamatsu and custom high speed counting electronics, both designed by Marina Photonics referred to as the PCount system. The initial unofficial specifications for the new counting electronics have indicated that the interface will be using RS-232 and/or Ethernet connection which has been accounted for in the redesign of the deck computer.

2.2 Laps Deck Computer

The original LAPS deck computer was based around the STD32 bus system with a Ziatech model ZT8902 486 processor board and uses a number of custom built cards as well as a few commercially available STD cards. A large portion of the time spent on this thesis involved determining the exact use and functionality of many of these cards. The only available documentation for many of the cards consisted of the schematics, many of which contained programmable logic chips for which no programming information was readily available. This resulted in having to reverse engineer to an extent many of these cards using what could be gathered from the schematics, usage in code, and the items connected to the cards which, if they were custom designed, were also not often completely functionally documented. For this reason the following subsections document the state of the signals as they are understood to exist in the original system in order to explain the choices made in the design of the new system and assist in debugging the new design. Figure 2.3 shows the existing deck computer layout and Table 2.2 shows the information for finding schematics of the various boards in the computer. Note that any unspecified references to “code” in this section refer to the “lapsdeck.cpp” code for the existing STD32 bus deck computer written by Dr. Daniel Lysak at ARL-PSU. In examining this code,

Table 2.1 showing the memory mapping used for the various cards may be useful. This table was created from the software and thus any naming used in the software is carried through here.

Table 2.1: Memory Map for Lapsdeck.cpp Software

Memory Address	Use In Program
0x1FF0	Radar control register
0x1FF1	Radar status register
0x1FF2	Radar blanking register
0x1FF3	Radar target range register
0xFC00	Timing card
0xFC03	Timing card digital delay chip values
0xFC04	
0xFC05	
0xFC07	Timing card sync
0xFC08	Digital interface card input port 0 (“board 1” in software)
0xFC09	Digital interface card input port 1 (“board 2” in software)
0xFC0B	Digital interface card output port (“relay board”)
0xFC0C	Digital interface card input port 2 (“board 3” in software)
0xFC11	Power relay driver board port 0
0xFC13	Power relay driver board port 1
0xFC60	Various analog card ports (usage not always clear)
0xFC70	
0xFC71	
0xFC7f	
0xFC90	The Versalogic electromechanical relay card

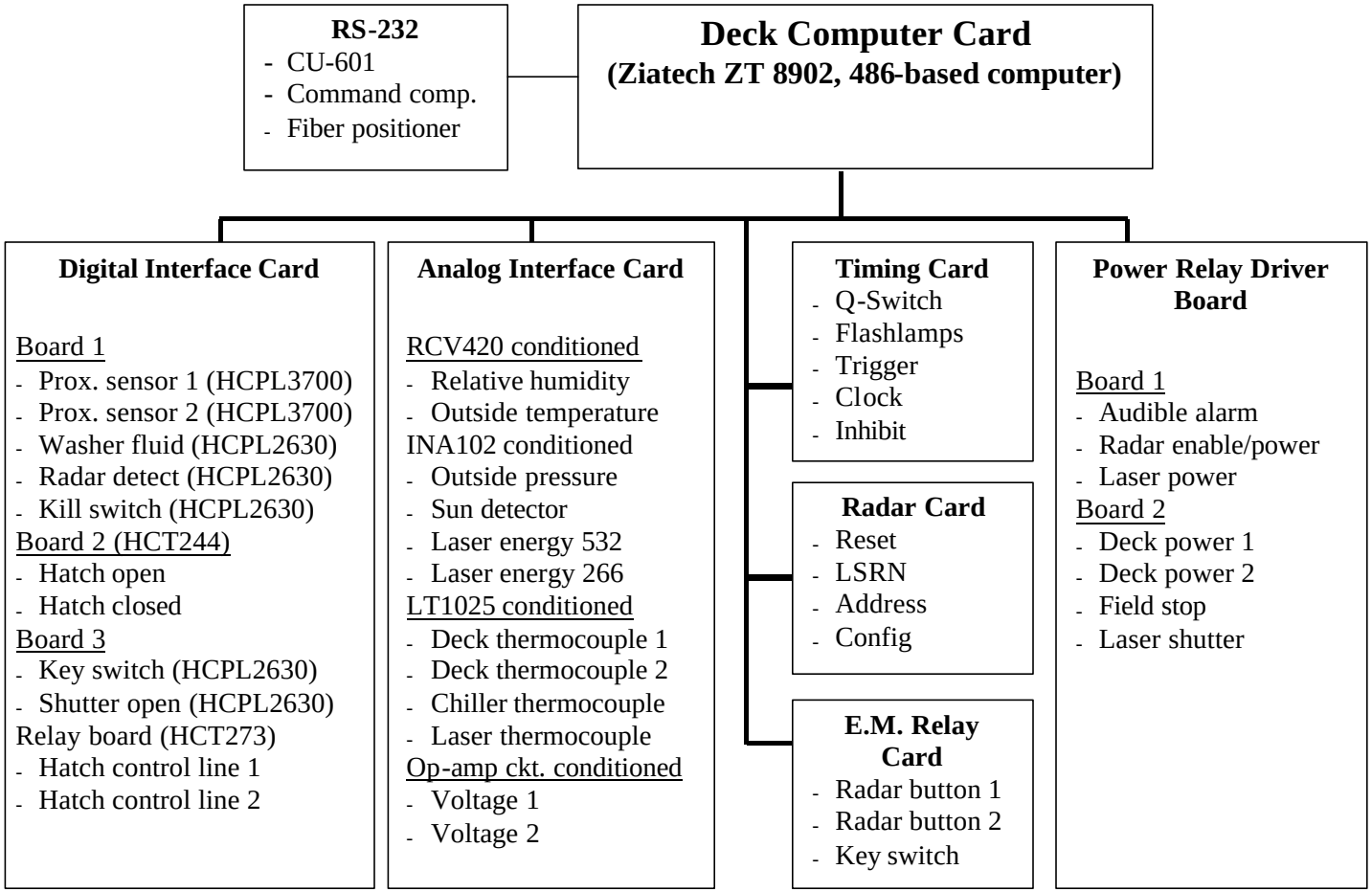


Figure 2.3: Existing Deck Computer Structure Block Diagram

Table 2.2: Signals From Original Deck Unit Computer

Signal Name	Type	External Conn. (Fig. 2.5)	Internal Conn. (Fig 2.3)	Logical Conn.	External Destination	Signal Description
Serial Port Interfaces						
Command Computer Link	RS-232	J1	Ziatech computer board	COM 1	Console computer via RS-232 fiber adapter	Provides the control link to the Console computer
CU601 Link	RS-232	J2	Ziatech computer board	COM 2	CU601 front panel	Provides control over CU601 for harmonic generator control and sends keep-alive signal
Fiber Position Control	RS-232	J11	Ziatech port expansion card pn. 88ZT65	COM 3	Oriel 18011 Motor Mike Controller	Controls the positioning of the telescope fiber
Electromechanical Relay Interfaces						
Radar Button 1	EM relay	J12	EM-RB	EM-RB (p0,b0)	Radar control panel	Simulates pressing of button to begin warming up radar
Radar Button 2	EM relay	J12	EM-RB	EM-RB (p0,b1)	Radar control panel	Simulates pressing of button to activate radar after 100 second warm-up
Key Switch	EM relay	loose wire	EM-RB	EM-RB (p0,b6)	Inside CU601, wired in parallel with key switch	Allows remote closing of key switch inside CU601
Power Relay Interfaces						
Audible Alarm	24VDC output	J14	PRDB	PRDB (p0,b0)	Terminal strip	Turns on power relay to sound audible alarm
Radar Enable	24VDC output	J14	PRDB	PRDB (p0,b3)	Terminal Strip	Turns on power relay to supply 24VDC to radar system

Signal Name	Type	External Conn. (Fig. 2.5)	Internal Conn. (Fig 2.3)	Logical Conn.	External Destination	Signal Description
Laser Power	24VDC output	J18	PRDB	PRDB (p0,b3)	Laser Power relay located near air conditioner	Turns on 220VAC to laser electronics rack. Note that this does NOT wire via the terminal strip as most do.
Deck Power 1	24VDC output	J14	PRDB	PRDB (p1,b2)	Terminal Strip	Turns on deck power relay 1
Deck Power 2	24VDC output	J14	PRDB	PRDB (p1,b3)	Terminal Strip	Turns on deck power relay 2
Field Stop	24VDC output	J16	PRDB	PRDB (p1,b4)	Directly to field stop solenoid	Drives the field stop solenoid
Laser Shutter	24VDC output	J16	PRDB	PRDB (p1,b5)	Wired to laser shutter in cavity	Drives the solenoid in the laser cavity
Digital Input and Output Interfaces (Non-relay)						
Hatch motor outputs(2)	5VDC to opto-iso.	J18	DIC (HCT244)	DIC	Compumotor SX/SXF controller	Drives the hatch motor and receives limit signals
Hatch motor inputs(2)	5VDC from opto-iso.	J18	DIC (HCT273)	DIC	Compumotor SX/SXF controller	Drives the hatch motor and receives limit signals
Proximity Sensor 1	110VAC digital input	J17	DIC (HCPL3700)	DIC (p0, b0)	Terminal strip	Connects via terminal strip to a motion sensor that turns on AC line voltage
Proximity Sensor 2	110VAC digital input	J17	DIC (HCPL3700)	DIC (p0, b1)	Terminal strip	Connects via terminal strip to a motion sensor that turns on AC line voltage
Deck Power	110VAC digital input	J17	DIC (HCPL3700)	DIC (p0, b2)	Terminal strip	Senses 110VAC on output of relay for deck power

Signal Name	Type	External Conn. (Fig. 2.5)	Internal Conn. (Fig 2.3)	Logical Conn.	External Destination	Signal Description
Washer Fluid Okay		J17	DIC (HCPL2630)	DIC (p0, b5)	unknown	This had been designed to sense the washer fluid level, but was unused at the time of the re-design.
Radar Digital Detect Signal	TTL 5V	-	DIC (HCPL2630)	unused	Internal signal, from radar card	Acts as a digital signal from the radar card in addition to its computer interface
Kill Switch	5VDC	J6	DIC (HCPL2630)	DIC (p0, b7)	To LAPS console	Current sensing loop. Will kill the laser if the circuit to the console kill switch is broken
Shutter Open	5VDC	J16	DIC (HCPL2630)	DIC (p4, b0)	To laser cabinet	Senses, by current, flow if shutter has actually opened
Analog Input Interfaces						
Relative Humidity	4-20mA	J15	AIC (RCV420)	AIC (line 1)	HX42	Senses external humidity
Outside Temp.	4-20mA	J15	AIC (RCV420)	AIC (line 2)	HX42	Senses external temperature
Outside Press.	0-5VDC	J15	AIC (INA102)	AIC (line 3)	Direct to pressure sensor	Sensed external barometric pressure
Sun Detector	0-5VDC	J15	AIC (INA102)	AIC (line 4)	Direct to sun sensor	Senses sun intensity from directly overhead
Deck Temp. 1	J-type T.C.	J7	AIC (LT1025)	AIC (line 8)	Thermocouple near laser cavity	Senses the internal ambient air temperature in the unit
Deck Temp. 2	J-type T.C.	J8	AIC (LT1025)	AIC (line 9)	Thermocouple in telescope	Senses the internal ambient air temperature in the unit
Chiller Temp.	J-type T.C.	J9	AIC (LT1025)	AIC (line 10)	Thermocouple in hose to chiller	Senses the temperature of the water coming from the external chiller

Signal Name	Type	External Conn. (Fig. 2.5)	Internal Conn. (Fig 2.3)	Logical Conn.	External Destination	Signal Description
Laser Temperature	J-type T.C.	J10	AIC (LT1025)	AIC (line 11)	Thermocouple in liquid probe in laser DI water tank	Senses the temperature of the water in the de-ionized water reservoir for the laser
532 Laser Energy	0-12 VDC analog	J16	AIC (INA102)	AIC (line 5)	Laser Energy monitor circuit in laser cavity	Senses the output of the laser energy monitor circuit for the 532 channel
266 Laser Energy	0-12 VDC analog	J16	AIC (INA102)	AIC (line 6)	Laser Energy monitor circuit in laser cavity	Senses the output of the laser energy monitor circuit for the 266 channel

For digital cards, (px; by) denotes port x, bit y.

Abbreviations:

EM-RB: Versalogic Electromechanical Relay Board
PRDB: Power Relay Driver Board
DIC: Digital Interface Card
AIC: Analog Input Card

Table 2.3: Deck Computer Card Schematic Files

Board	ARL file#	ARL Project Title
Lidar Digital Interface Card	7523.0015	Lidar digital interface card
Analog Input Card	7523.0015	Lidar LAPS project analog input card
Timing Board	7523.0115	Lidar LAPS project laser data acquisition/timing board
Radar Interface Card	7523.0115	Lidar LAPS project radar interface card
Power Relay Driver Card	7523.0015	LAPS lidar power relay driver board
Electromechanical Relay Board	Not applicable, this is a commercial card, Versalogic pn 2312	

2.2.1 Digital Interface Card

The deck computer Digital Interface I/O card was initially one of the more difficult to understand due to the way in which it is referenced in the lapsdeck.cpp software. It is believed that during the early design of the software that multiple cards existed and the separate "board" names were simply carried over. The board is referred to as four separate boards in the lapsdeck code which are essentially the four different memory mapped byte ports of the one board. "Board #1" and "Board #3" are connected to either HCPL3700 or HCPL2630 inputs as listed in Table 2.2, "Board #2" is an input through an HCT244 IC, and the "relay board" uses an HCT273 IC for output. A brief description for each of these types of ICs is provided in Table 2.4 below.

Table 2.4: Digital Interface Card ICs

Digital Interface IC	Description
CD74HCT244	TTL level input buffer
CD74HCT273	TTL level output buffer
HCPL2630	Optically isolated inputs for DC current. 5mA input turn-on current, 15mA max, 7 VDC max, 100ns propagation delay [1]
HCPL3700	Optically isolated inputs for 5 to 240 VAC/DC input sensing, 50mA max average current, 40µs max propagation delay [2]

2.2.2 Analog Input Card

The analog input card is designed to be used to condition and sample various analog inputs from the system. Based on the lapsdeck.cpp software, the conversion cycle time used for this card was approximately 5ms per channel. Though this seems somewhat slow, it should be noted that none of the analog data to be sampled should be changing at any significant rate, thus a low sampling rate is appropriate to save on processor usage. The only case in which this was not entirely clear is that of the laser energy monitor, where the software appears to attempt to synchronize with the laser firing; however, this is unnecessary as the energy monitors use a circuit to provide a DC output proportional to the laser output power. The various types of analog inputs such as current, voltage and thermocouple inputs are conditioned by onboard ICs in a custom board which provides a compact but extremely inflexible design.

Table 2.5: Analog Conditioning ICs

Analog Conditioning IC	Description
RCV420	Converts 4-20mA signals to a 0-5V signal [6]
INA102	Differential voltage input supporting x1 to x1000 gains set by wire wraps on the board [5]
LT1025	A chip which converts a J type thermocouple signal to a 0-5V signal.

2.2.3 Relay Driver Card

The power relay driver card is primarily used for activation of solenoids or the control of larger AC power relays for the main power systems by switching an external 24VDC power supply. Referred to as “relay board #1” and “relay board #2” in deck code, all outputs are via IRFF130 MOSFETS. The output MOSFETS are labeled as

IRRF123s in the ARL schematic, however this is incorrect. A search for specifications on an "IRRF123" part number without finding any references leads one to believe this was a labeling error rather than a design change between types of MOSFETS. The IRFF130s are 8A, 100V, 0.180Ω impedance devices that are essentially similar to solid state relays[14]. Since it seemed unlikely that multiple 8A currents were being brought onto the board over 22-26 gauge wire, a number of the current levels such as the deck power relays and the audible alarm were measured and found to be in the 100mA to 200mA range. On this board, signals through buffer IC "U2" on the schematic are port 0, signals through buffer IC "U3" are port 1.

2.2.4 Electromechanical Relay Board

The electromechanical relay board referred to as relay board FC90 in the deck code is actually a Versalogic part number 2312, most likely named due to its memory address being 0xFC90. The information printed on the card gives the following output capabilities: 24VDC@1.25A, 24VAC@1.25A, 100VDC@0.3A, and 120VAC @0.5A. For our purposes, the primary difference between the MOSFETS or solid state relays, and electromechanical relays should be noted. When a typical solid state relay is "closed" a specific amount of current through the output is required to allow it to maintain its closed state or it will turn off. An electromechanical relay does not have this requirement, hence is more suitable for actions such as wiring in parallel with buttons or switches which may not have the required current provided to maintain the relay in the closed state.

2.2.5 Data Acquisition and Timing (DAQ) Card

Before reading this subsection, it will be useful to have the Continuum manual for the Powerlite 9000 series lasers available[9], in particular Chapter 2 section E regarding direct access triggering should be well understood. While procedure followed in the LAPS design does not exactly follow the procedure in the book, the timing and logic are the same. The primary difference is that the Q-Switching signal is input across pins 5 and 9 of the "Externals" connector. The CU601 has been modified internally such the internal connection which was the "external Q-sw in" input on the CU601 back panel is now wired to these two pins. The DAQ card provides the flash lamp and Q-Switch outputs as specified in the Continuum manual. It also provides trigger, clock, and inhibit signals to the CAMAC electronics in the Console. The main function of this card is to allow the laser Q-switch pulse to be synchronized with the trigger and clock of the CAMAC so that altitudes can be assigned correctly and consistently to photon counts. Programming information for the programmable logic on the DAQ card was not available and some operational details are not entirely clear; however, the important functionality and timing constraints for this card are well understood. The card provides a 500ns width dwell clock output for a period after sending a trigger signal which is the fastest that the CAMAC averaging unit can respond to [12] and results in our 75 meter vertical "bins" from the equation:

$$\overbrace{500\times10^{-9}\,\text{seconds}}^{\text{dwell clock}}\times\frac{\overbrace{3\times10^{8}\,\text{meters}}^{\text{speed of light}}}{\text{second}}\div\underbrace{2}_{\text{photon goes up and comes back down}}=75\,\text{meters}$$

At a rate of 30 Hz, it also supplies a TTL flashlamp triggering which starts the laser pulse and data acquisition cycle shown in Figure 2.4. At a time $t_{fl\text{-}qsw}$(roughly

200μs) later, the card sends out a Q-switch pulse which will cause the laser pulse to be emitted some $t_{qs\text{-}le}$ (roughly 80ns later)[9]. For both $t_{fl\text{-}qsw}$ and $t_{qs\text{-}le}$ the exact time spans are not critical, however their difference must have very low jitter, less than 5 ns or 1% of an altitude bin, to provide consistent altitude correlation to received photons. The critical timing for the system is relating the time of the laser's pulse output from the exit window to the start of a known CAMAC data bin after the trigger. The CAMAC Averager will report the first clock "bin" occuring more than 50nsec after a rising trigger edge as the first data bin[12]. This timing is provided by having precise control of the Q-switch timing relative to the flashlamp pulse which is the start of the cycle. Since the flashlamp pulse occours a fixed amount of time before the CAMAC trigger this gives the needed delay adjustment. Adjustment of this timing is accomplished with a combination of wire wrapping on the board as a coarse setting (500 ns per step) and by three cascaded digital delay generators (Dallas Semiconductor DS1020-50)* which can each theoretically add from 0ns to 128ns of delay set via software in 0.5 ns increments. In reality, due to the width of the generated pulse each digital delay generator may only be used to generate roughly 50ns of delay[13]. Note that in Figure 2.4, the clock is shown as a patterned area indicating many thousands of clock cycles occur in this region corresponding to the bins of data.

* Dallas Semiconductor is now a subsidiary of Maxim Integrated Products.

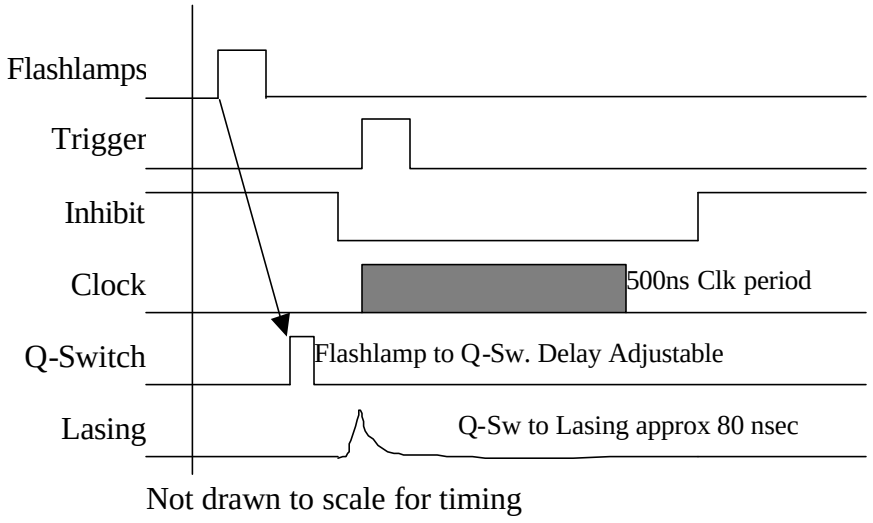


Figure 2.4: Timing Card Timing Diagram

The typical procedure for setting this delay involves placing a fast rise photodiode on the exit hatch of the LAPS unit pointing towards the exiting beam. A 400MHz+ oscilloscope is then triggered off the synch signal from the CB634H J4 connector. Two channels of the scope then observe the outgoing pulse of the laser and the trigger into the CAMAC respectively. The trigger should be occurring approximately one or two "bins", or 500ns increments, before the pulse photons would be entering the counters. Assuming only a two channel display scope is available, the scope should now be set to trigger off of the falling edge of the trigger signal so that the laser pulse and the clock input to the CAMAC can be observed. The pulse should be timed using the Q-switch timing adjustments so that the observed peak will occur just after one of the clock rising edges, typically the 2^{nd} or 3^{rd}. Which bin clock edge is not important since the starting bin of the CAMAC to use as real data can be specified in the console software.

It should be noted that much detail was omitted in this section related to the notion of "shifting" the pulse in time to account for delays. In this procedure, the wire length delays of the test BNC cables must be taken into account and compensated for as well as many other factors. Appendix D provides a Matlab program used in the Summer of 2001 which attempts to take into account the necessary shifts for a true correction. This description motivates the plan for switching to a method which triggers off of a photodiode which iss planned for ALAPS as described in Section 3.3.

2.2.6 Radar Interface Card

The radar interface card, designed by Scott Boone, is very well documented in his thesis "A Digitally Controlled Safety Radar Subsystem for Atmospheric Lidar Systems" [4] and thus will be discussed only briefly here to provide the details that are necessary for this thesis. The purpose of this STD32 card is to take the signals from the modified Raytheon marine radar system and provide an automated cutoff of the laser transmitter. The current usage is to poll the card for status and, if a detection has been observed, to close the shutter and stop the Q-Switch signal generated by the timing card. It should be noted that the timing sequence of this card and the electromechanical relay "button" pressing for the radar panel need to be done in a specific sequence.

2.2.7 Deck Computer Internal Wiring

The connectors shown in Figure 2.5 are described in Table 2.6 accompanied by pin descriptions for each custom connector in Tables 2.7 to 2.12. The majority of the information in these tables is a composite of information from schematics in the "Lidar Support" package combined with references in the lapsdeck.cpp source code. The code

helped establish the function of some wires which were not in the schematics. In addition it should be noted that no complete diagram such as Figure 2.4 above could be found to match schematics to physical connectors, thus many references to connectors in this section are slightly different than the references in the schematics.

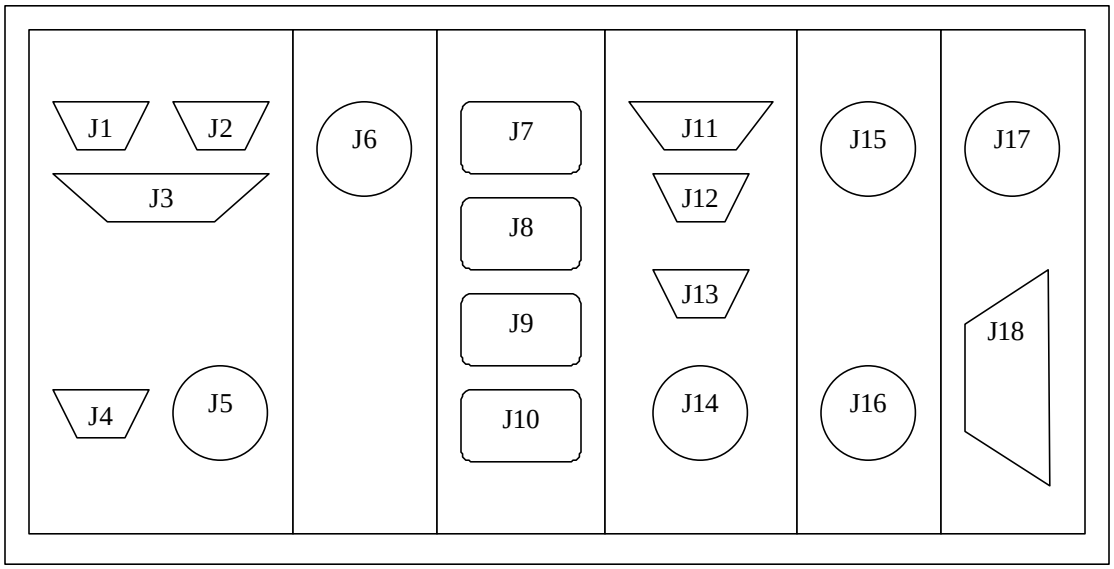


Figure not to scale

Figure 2.5: Layout of Original Deck Computer Faceplates

Table 2.6: Original Deck Computer Faceplate Connector Descriptions

Connector	Description
J1	COM 1 (Console link)
J2	COM 2 (CU601 link)
J3	LPT 1 (unused)
J4	STD bus monitor out
J5	AT-style keyboard connector
J6*	Timing card output to console and CU601 externals (see table 2.7)
J7	J-Type thermocouple input for deck temperature 1
J8	J-Type thermocouple input for deck temperature 2
J9	J-Type thermocouple input for laser DI water temperature
J10	J-Type thermocouple input for chiller water temperature
J11	COM 3 (Fiber motor controller)
J12*	DB-25 for mechanical relays to radar system (see table 2.8)
J13	DB-9 signals from radar system to radar card (see Scott Boone thesis)
J14*	Primary connection to power relay driver card (see table 2.9)
J15*	Analog input from terminal strip (see table 2.10)
J16*	Analog input from laser (energy monitors). power for energy monitors and connection to relay driver card for laser shutter (see table 2.10)
J17*	Digital inputs from terminal strip (see table 2.11)
J18*	Hatch motor connections (see table 2.12)
* Pin descriptions given in separate table	

Table 2.7: Pin Description for Original Deck Faceplate J6

Pin	Wire Color	Internal Connection	Function
1-16	Multicolor ribbon cable	Ribbon cable to timing and data acquisition card	These are wired to the 16-conductor ribbon cable from the timing card in order
17-51	No Connection		
52	Red	DIO card J2-31	Status of current loop for kill switch from console.
53	Black	DIO card J2-30	
54	Red	+5V from aux. power supply	These are wired to the CU601 externals connector and are used as the charge “signal”
55	Black	GND from aux. power supply	

Table 2.8: Pin Description for Original Deck Faceplate J12

Pin	Wire Color	Internal Connection	Function
1	Orange	EM relay 0	Radar Button 1
2	Yellow	EM relay 0	
3	Brown	EM relay 1	Radar Button 2
4	Blue	EM relay 1	
5	White	Tied together internally, unused	
6	Black		
7	Red		
8	Green		
9	Yellow	Ends not connected, unused	
10	Orange		
11-25	Not Connected		

Table 2.9: Pin Description for Original Deck Faceplate J14

Pin	Wire Color	Internal Connection	Function
A	Yellow	J2-22 (+24VDC bus on card)	+24VDC Supply
B	Black	J2-34 (Ground bus on card)	+24VDC Supply common
C	Black	J2-6	Unused Power Relay Driver
D	Gray	J2-23 (+24VDC bus on card)	
E	Gray	J2-7	Radar power enable
F	White	J2-24 (+24VDC bus on card)	
G	Purple	J2-8	Unused Power Relay Driver
H	White	J2-25 (+24VDC bus on card)	
J	Brown	J2-9	Unused Power Relay Driver
K	White	J2-26 (+24VDC bus on card)	
L	Orange	J2-10	Audible Alarm
M	White	J2-27 (+24VDC bus on card)	
N	Green	J2-13	Deck Power 2
P	White	J2-30 (+24VDC bus on card)	
R	Blue	J2-14	Deck Power 1
S	White	J2-31 (+24VDC bus on card)	
T	Brown	J2-15	Unused Power Relay Driver
U	White	J2-32 (+24VDC bus on card)	
V	Yellow	J2-16	Unused Power Relay Driver
W	White	J2-33 (+24VDC bus on card)	
X-Z a-c	Not Connected		

- This table is based off of the “Relay Wiring Diagram” from the Lidar Support packet of drawings, file # 7523.0093
- All “J2” references refer to J2 on the Power Relay Driver Board.
- Relay function was determined using the port and bit number from Appendix A along with the Power Relay Board schematic.
- Pin A goes to the J2-22 Relay Board connection via a time delay fuse as a yellow wire which exits the fuse as an orange/pink wire to J2-22

Table 2.10: Pin Description for Original Deck Faceplate J15

Pin	Wire Color	Internal Connection	Function
A	Purple	J2-13	Relative Humidity Sensor
B	Yellow	J2-31	
C	Not Connected		
D	Gray	J2-33	Outdoor Temperature Sensor
E	Yellow	J2-14	
F	Not Connected		
G	Orange	J2-16	Pressure Sensor
H	Purple	J2-34	
J	Not Connected		
K	Black	J2-17	Sunlight Detector
L	Brown	J2-35	
M-V	Not Connected		

- This table is based off of the "Analog Wiring Diagram" from the Lidar Support packet of drawings, file # 7523.0093
- All "J2" references refer to J2 on the Analog Input Board

Table 2.11: Pin Description for Original Deck Faceplate J16

Pin	Wire Color	Internal Connection	Function
A	Red/Pink	Supply +12VDC (tied to K)	Power for energy monitors
B	Green	Supply Common (tied to T)	
C	Black	Supply –12VDC (tied to S)	
D	Red	Power Relay Board J2-29	+24VDC supply for field stop
E	Brown	Analog Input Board J2-18	Laser Energy Monitor Input
F	Blue	Analog Input Board J2-36	
G	Not Connected		
H	Yellow	Analog Input Board J2-19	Laser Energy Monitor Input
J	Gray	Analog Input Board J2-37	
K	Red/Pink	Supply +12VDC (tied to A)	Unknown
L	Yellow	Analog Input Board J2-2	Window Monitor
M	Orange	Analog Input Board J2-21	
N	Not Connected		
P	Blue	Splits to: Relay Driver Board J2-17 DIO Board J2-6	Power for laser shutter and signal for DIO card
R	Black	Power Relay Board J2-12	Return to relay for field stop on power relay driver board
S	Black	Supply –12VDC (tied to C)	Unknown
T	Green	Supply Common (tied to B)	Unknown
U	Black	Splits to: Relay Driver Board J2-11 DIO Board J2-7	Return to relay for laser shutter on power relay driver board and connection to DIO current sensor

- This table is based off of the "Analog Wiring Diagram" from the Lidar Support packet of drawings, file # 7523.0093
- The pins P and U seem to wire a current sensing input of the DIO card in PARALLEL with the laser shutter solenoid which seems unusual.

Table 2.12: Pin Description for Original Deck Faceplate J17

Pin	Wire Color	Internal Connection	Function
A	Green	J2-12	Roof proximity sensor
B	Red	J2-13	
C	Green	J2-14	Side proximity sensor
D	Orange	J2-15	
E	Blue	J2-16	Deck Power from relay #3
F	Green	J2-17	
G	Red	J2-18	AC Heater Power (This is unused in lapsdeck.cpp)
H	Orange	J2-19	
J	Blue	J2-22	Radar Power
K	Red	J2-23	
L	Blue	J2-24	Washer Level Sensor
M	Red	J2-25	
N-Z a, b	Not Connected		
c	Black	J2-5	DIO Common

- This table is based off of the "Digital Wiring Diagram" from the Lidar Support packet of drawings, file # 7523.0093
- All "J2" references refer to J2 on the Digital Input Board.

Table 2.13: Pin Description for Original Deck Faceplate J18

Pin	Wire Color	Internal Connection	Function
1	Green	DIO Board J2-37	
2	Yellow	DIO Board J2-39	
3	Orange	DIO Board J2-41	Brown wire to hatch controller “I2”
4	Yellow	DIO Board J2-44	
5	Blue	DIO Board J2-46	
6	Red	DIO Board J2-48	
7	Red	DIO Board J2-50	Orange wire to hatch controller “CW”
8-12	Not Connected		
13	Red	Relay Driver Board J2-23	Laser Power Control +24V
14	Yellow	DIO Board J2-38	
15	Purple	DIO Board J2-40	
16	Red	DIO Board J2-42	Black wire to hatch controller “I1”
17	Orange	DIO Board J2-45	Green wire to hatch controller Ground
18	Green	DIO Board J2-47	
19	Green	DIO Board J2-49	
20	Orange	DIO Board J2-51	
21	Blue	DIO Board J2-52	Blue wire to hatch controller “CCW”
22	Red		Red wire to hatch controller “OPTO1” and “OPTO2”
23, 24	Not Connected		
25	Black	Relay Driver Board J2-5	Laser Power Control

- This table is based off of the “25-Pin ‘D’ Wiring Diagram” from the Lidar Support packet of drawings, file # 7523.0093

2.3 LAPS Deck Unit Subsystems

In order to understand some of the design choices, a brief background on the remainder of the deck unit is necessary. As the majority of the subsystems discussed are commercially available items, only a very brief description is given while details are

available in the product manuals. Some analysis of the timing requirements or safety requirements associated with each component will also be given as necessary.

The first of the items to be discussed is the laser control unit, or CU601. This unit provides some basic status information on the operation of the laser as well as allowing control of the harmonic generator crystals via an RS-232 connection. In addition, this unit accepts the timing signals as described in section 2.2.5 concerning the data acquisition and timing card[9]. The second item, also controlled over an RS-232 interface, is the Oriel 18011 Motor Mike fiber positioner for the telescope receiver. This system allows the fiber to be aligned and positioned at the focal point of the receiving telescope[16].

Another major subsystem of the deck unit is the radar system which is a modified Raytheon marine radar. This safety system is activated via both the radar card described in the thesis of Scott Boone and two relays which allow remote “pressing” of buttons. It should be noted that these relays must be electromechanical relays rather than solid state relays due to the fact that most solid-state relays require a minimum load current to remain in the “on” state.

The system collectively referred to as the “Environmental Sensors” package is a set of instruments designed to measure external temperature and humidity (Omega HX42), external atmospheric pressure (Viatran Model 246), sunlight intensity, and interior temperatures of the deck unit using a number of thermocouples. Each of these is an analog input and their interface is described in Table 2.2.

The last major electronic subsystem in the deck unit is the hatch motor controller, which is a Compumotor SX/SXF Indexer/Drive. This is interfaced to in the existing

deck system via TTL logic signals which seems to contradict the suggested interface method given in the manufacturer's manual where a detailed description of the interface is given. This subsystem also is considered to encompass the linear actuator and sensors used in the hatch[8].

Chapter 3: New LAPS Deck Computer Design

The goal of this chapter is to explain the basic high level design decisions made in the upgraded system while detailed wiring, physical layout and other lower level information will be discussed in Chapter 4. In order to meet the flexibility requirements for changing over to a research and development system rather than a static prototype design, one of the first things determined to require updating is the control computer. The existing LAPS deck computer, while having some amount of flexibility in its STD32 bus design, has a number of major drawbacks. The first of these being that the STD bus is becoming obsolete and s being replaced by standards such as Compact-PCI, PC/104 and others. In addition, the STD bus cannot interface with normal PCI or ISA cards while most newer standards have adapters for such conversions readily available if needed. Next, the cards for digital I/O, which includes the power relay driver card, are custom made to handle specific types of signals which violates the COTS design principle and drastically reduces flexibility. Those digital signals that deal with AC power also, in some cases, bring 120VAC onto the cards which leads to dangers from surges and noise. A similar issue is seen with the analog input card which uses on-card signal conditioning and provides little protection from noise and surges, while almost eliminating the ability to modify the types of inputs. It should once again be noted that the issues of flexibility, noise isolation, and off the shelf design were not as important given the original system design goals, thus these shortcomings are much more the result of changes in goals and intended usage rather than incorrect past design choices. In addition, in this electronic design, no MIL-SPEC requirements were considered as design requirements; however, this is perfectly reasonable considering the laser itself

cannot meet many MIL-SPEC requirements and will be subjected to the same conditions as the deck computer.

Another major issue is that the existing LAPS design does not have the capability of providing hard real-time safety guarantees while providing the services that will be required in ALAPS, namely data serving and data acquisition from the CAMAC or PCount systems. As will be discussed later, the choice of RT-Linux will allow this on a reasonable system. It can be argued that multiple computers could be used to meet this goal, a simple computer providing real-time safety and another "server" computer for data acquisition; however, this introduces another point of failure into the system while unnecessarily increasing complexity. Despite this point, to meet the goal of not jeopardizing any significant safety features, it will be seen that as a temporary measure an approach similar to this was forced.

Finally, it is desired to move away from the fairly unreliable RS-232 communications between the console and deck computers. IP communications over Ethernet provides an ideal setup where communications can be done remotely over the network and all line error checking is handled by the underlying system ensuring fewer link failures which have been a serious problem with the existing system. TCP/IP also provides the ability for serving data using FTP or other methods making it an even more ideal approach. The old computer does not have the resources to effectively make use of TCP or UDP protocols.

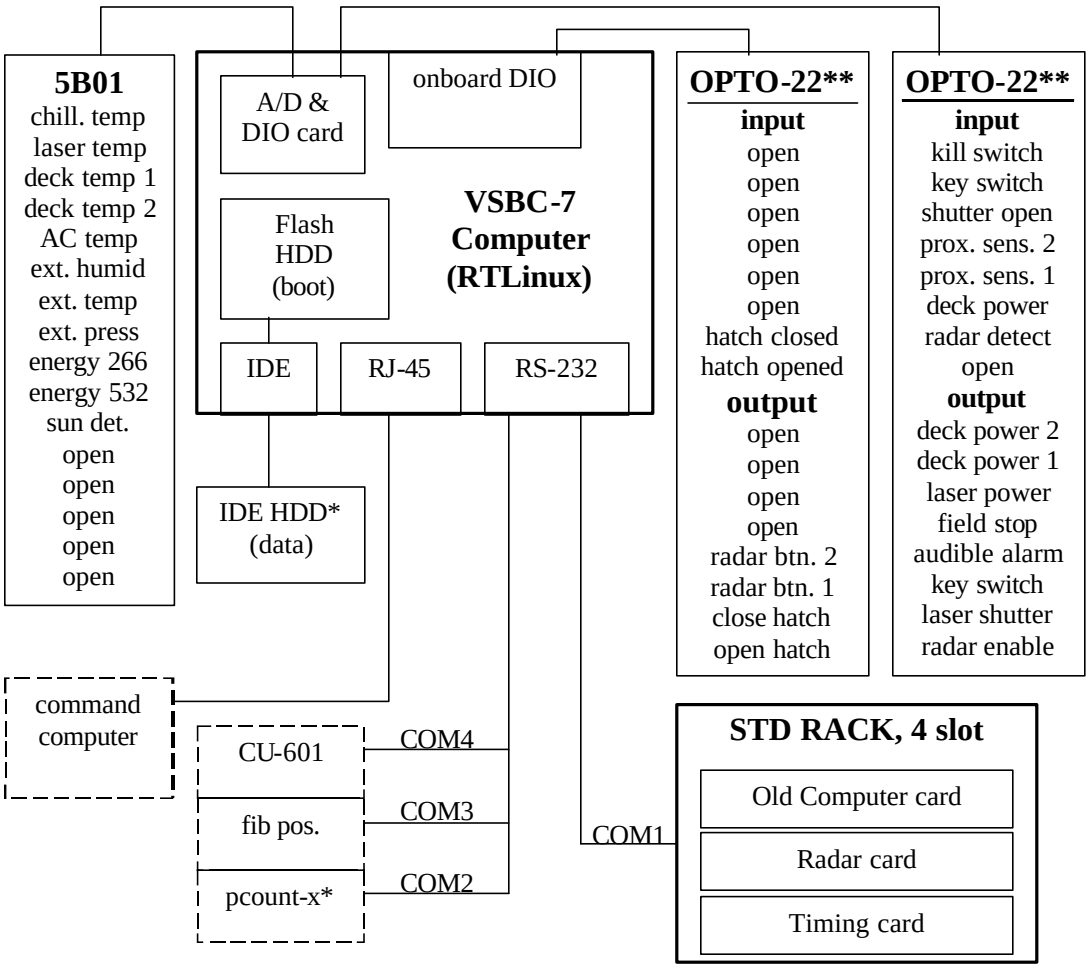
In designing the new deck computer a number of considerations were made and constitute the design goals:

- Retain all existing functionality

- Provide for a connection to proposed new internal counting hardware (RS-232 command & Ethernet for data), as well as computer resources for in-unit data acquisition, processing, storage and serving
- Make the system as flexible as possible for use as a research tool and test-bed
- Keep space within the existing 19”W x 24”D x 7”H volume [*]
- Provide remote control via TCP/IP connection rather than RS-232
- Use COTS parts as much as possible for items which will transfer to ALAPS
- Attempt to keep the hardware cost under $6,000 total, preferably well under
- Do not modify or jeopardize any safety features which cannot be easily re-verified

The overview of the chosen design for the computer is shown below in Figure 3.1 and will be explained through the remainder of this chapter.

[*] Due to time constraints, the physical design was begun before the existing system was removed. Because of this, the exact layout of components inside the rack mount was not completely understood. In reality the available space was approximately 19”W x 21”D x 6.5”H.



* Not currently installed, for use when data acquisition is moved to the deck unit.
** OPTO-22 modules listed from module 0 up to module 15

Figure 3.1: Overview of New Deck Computer

3.1 Choice of Computer Standard

The choice between standards for the computer was one of the more difficult design points as there were many different formats which would meet the goals. All formats which required a back plane and cards such as PISA and PICMG had the disadvantages of being larger and more expensive, but were more flexible as any standard PCI or ISA cards could later be used in the rack. PC/104 was far smaller with

all the necessary functionality on an EBX format board and one PC/104 module, but required an adapter for using standard PCI or ISA cards. It also provided less inherent physical protection due to the lack of a card cage. Thus, the type of future flexibility required needed to be questioned and it was decided that the flexibility provided by the 5B analog signal conditioning modules and digital conditioning modules would be sufficient. The system still provided for two additional PC/104 cards which could be added later. In addition, the PC/104 format would allow the rack mount chassis to be reduced in height to as little as 3.5" in the future if necessary with only minor changes. The board chosen was the Versalogic VSBC-7 due to its fast processor, onboard OPTO-22 compatible DIO, onboard RJ45 Ethernet and four onboard RS-232 ports[19]. Versalogic was chosen due to the fact that they also are a source for the few needed STD32 products and it was preferred to go with a single provider.

3.2 RT-Linux Overview

The choice of operating system was one of the simpler decisions in the design of the system. The operating system had to provide a hard real-time capability for safety related signals, the ability to easily handle TCP or UDP over IP with little additional software, common programs such as FTP servers or WWW servers for data distribution, and finally could not contribute greatly to the overall cost. RT-Linux achieves all of these goals.

At this point, the term "real-time" should be clarified as well as how it relates to our needs. A real-time operating system is a system that provides some sort of guarantee about its interrupt response time regardless of non-real-time system load. A "soft" real-time system is one that essentially states that it will *typically* respond in the

specified amount of time, while a “hard” real time performance guarantee means that the timing will be met *100%* of the time, which is what is necessary for a safety system. The important safeties to respond to are the system “kill switch” and the radar system. The kill switch is a mechanical switch which is hit by a user to bypass the console computer and immediately stop the laser emissions. Since a typical person would take at least a second to pick up and hit such a switch, a real time response on the order of a hundred milliseconds should be acceptable. On the other hand, the radar system is designed to shut off the system automatically in the event of a plane fly-by. From the thesis of Scott Boone[4], on p19 it can be seen that a 50 millisecond response time can be considered a reasonable maximum time from the plane entering the radar cone to the beam shutoff. A reasonable limit for the response time of the operating system to this event should then be on the order of approximately 1 millisecond which will at worst cause one less pulse of the 750Hz PRF radar to be available to act upon.

The chosen operating system, RT-Linux, provides for all of these conditions while making available all the capabilities of the Linux operating system. The RT-Linux operating system is distributed and maintained by FSMLabs and has been gaining popularity as a free (GPL) competitor to other real time operating systems. The essential idea of RT-Linux is to slip a small real time operating system behind the Linux operating system and then run Linux as a low priority thread. This allows Linux applications and the system to function normally but always allows the real time functionality to interrupt when necessary. The performance of this method is extremely good providing less than a 20 microsecond response to an external interrupt, which is more than sufficient for our needs[18]. Thus even while processing acquired data, or

providing data to networked computers, timely response to timing requirements and safeties is guaranteed.

When stating the response time of a real time OS it should be noted that the response is typically to an interrupt request assertation such as that generated by an onboard timer or other card. In the current design of the system software, the cycle of reading the various inputs is *not* done based on interrupts but on RT-Linux thread "sleeping" functions which cause the thread to periodically "wake up" and sample the inputs, make time-critical decisions and pass the data on to the user-mode program. This "waking up" of the thread even without using interrupts preempts all other operating system functions and thus essentially provides the same ability to put time critical responses first. If desired, the VSBC-7 does include a number of hardware timers capable of generating interrupts at a periodic rate[19]. This may become useful for control systems such as the proposed horizontal scanning mirror for the system where positional sensors need to be updated at a highly predictable rate.

3.3 Handling of Radar and Timing Cards

One of the more disappointing points of this design is the temporary method in which the carry-over of the radar and timing cards was forced to be carried out. Due to both time and budget constraints, the existing STD cards were reused along with the processor card in a stripped down four-slot STD rack. This was done primarily because insufficient time was available for providing a full test of a newly designed radar card which must function perfectly as it is a critical safety point. The timing card redesign would not have been difficult given additional time (see Appendix B), however priority was given to ensuring the correct implementation of the critical basic systems. Another

point to be noted is that neither the timing nor radar cards will likely be necessary in the final ALAPS design. This is because the 3rd harmonic of the 1064nm ND-YAG laser, or 355nm, will be used and the beam will also be further expanded. Viewing a reflection of such a beam for brief periods, such as reflections from a metal surface, is well into the eye safe levels[10]. Due to the fact that the radar operation requires using the Versalogic 2312 relay card to "press" radar panel buttons in sequence with sending commands to the radar card, the STD computer provides control signals to the SBC over its serial link.

It is anticipated that in ALAPS, the timing card will be unnecessary since the PCount electronics require only a single trigger signal signifying the start of data acquisition for the laser pulse rather than an external clock and trigger as needed by the existing CAMAC system. This trigger can be provided by a fast (about 1ns) photodiode in the laser cavity. The timing of this system can be illustrated as in Figure 3.1 below.

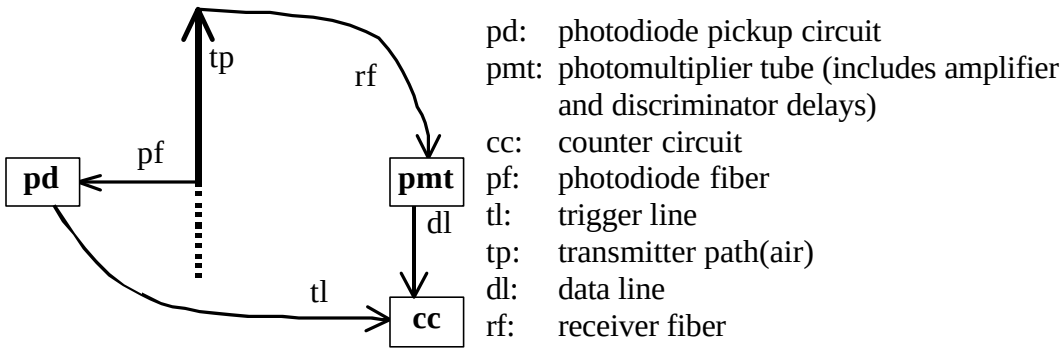


Figure 3.2: Timing of P-Count off Photodiode Trigger

From this diagram, the amount of missed data in meters is related to the amount of time from when the first counts from the PMT arrive at the counting electronics to

the time the counting electronics respond to the trigger and is given by,

$$M = c \cdot \left(\left(\frac{l_{pf}}{s_{pf}} + d_{pd} + \frac{l_{tl}}{s_{tl}} + d_{cc} \right) - \left(\frac{l_{tp}}{c} + \frac{l_{rf}}{s_{rf}} + d_{pmt} + \frac{l_{dl}}{s_{dl}} \right) \right)$$

where l_x is the length of item x, s_x is the propagation speed in item x, and d_x is the delay of item x. If the following assumptions are made: c=3e8 m/sec, l_{pf}=0, d_{pd}=5ns, l_{tl}=l_{rf}=2m, d_{cc}=25ns[15], l_{dl}=1m, s_{pf}=s_{rf}=0.7c, s_{dl}=s_{tl}=0.6c,d_{pmt}=6ns; the resulting missed data interval is,

$$M = c \cdot \left(\left(\frac{0}{0.7c} + 5e^{-9} + \frac{2}{0.6c} + 25e^{-9} \right) - \left(\frac{3}{c} + \frac{2}{0.7c} + 6e^{-9} + \frac{1}{0.6c} \right) \right) \approx 3m .$$

Due to the form factor of the receiver telescope, data below 20m is essentially useless because of low count rates making this three meter loss completely acceptable. Despite this rationale, producing a new combined radar and timing card will be advantageous should the system be used for an extended period of time with the current electronics and at the 2nd harmonic, therefore some preliminary design information on such a combined card is given in Appendix D.

This having been noted, the solution adopted was to allow the reduced STD32 bus computer to communicate with the new deck computer over a serial link. Despite the slowness of the serial communication, the radar safety timing is still maintained at its original level. This is due to the fact that the timing card is also on the STD bus computer and can therefore be commanded to stop the Q-switching signals, thus cutting off the beam while a small delay will elapse before the actual deck computer is able to close the shutter.

3.4 Interfaces to Deck System

The choice of the interface "buffer" between the actual laps deck and the computer was a major change from the design methodology of the old computer. In this new design, virtually no signal goes directly from a computer board to the system without going through a signal conditioning module, while in the old system all conditioning was done on the computer cards. This approach has the advantages of providing isolation from system surges or noise, allowing use of all commercial hardware, and greatly increasing system flexibility. The only disadvantage to this choice is that the size of the module racks is much greater than the implementation using a custom board; however, the reductions in size of other parts of the system permit the advantages of the modular signal conditioning to more than offset the size increase.

3.4.1 Analog Input 5B Modules

For the conditioning of analog signals, the 5B series of signal conditioning modules from Analog Devices were utilized. The usage of these modules added greatly to the overall cost of the system at roughly $130 per module; however, given their hardware linearization of inputs, surge isolation of 1500Vrms, noise filtering capabilities, and the ease with which they allow changes in system configuration the cost was deemed worthwhile. Each of the modules is designed to accept some type of input such as voltage, current or a thermocouple and output a scaled -5V to 5V signal which is appropriate for an ADC[3]. Essentially, this rack serves as a replacement for the analog interface card's interface IC's in the old deck computer. The rack used was a 16 channel model 5B01. The modules used depend on the type of input and are listed

below in Table 3.1. Full documentation for the Analog Devices parts may be found on their web site at http://www.analogdevices.com/.

Table 3.1: 5B Analog Conditioning Modules

Module Description	Module Model	Signals Used With
0 to 20mA input	5B32-01	outside temperature outside humidity
-5V to 5V input	5B31-05	outside pressure sun detector power monitor 266 power monitor 532
J-Type thermocouple	5B37-01	chiller temperature laser temperature
RTD input 100Ω Platinum 0°C to 100°C	5B34-02	deck temperature 1 deck temperature 2 AC temperature

3.4.2 Digital Input and Output Conditioning Modules

The concepts behind the use of the digital IO modules are similar to the analog modules in that they provide easy system modification, isolation from the high power of the system and conditioning of inputs. However, the decision to use these modules was made much easier due to their extremely low cost, roughly $15 per module. A wide variety of modules is available for use from OPTO-22, the chosen supplier. OPTO-22 was chosen primarily because the Versalogic boards specifically listed pin compatibility with their PB16H racks[19][20]. To accommodate the necessary number of signals, two PB16H 16 module racks were used with G1 modules. While higher density racks are available this would have required custom cabling since our DIO ports were each only 16 bits and custom cabling goes against our COTS philosophy even though it would not likely be complicated. G4 modules also could have been used to reduce

space slightly at a slightly higher cost. "Bussed" module racks are also available from OPTO-22 which allow multiplexing more than 16 modules onto a 16 bit port; however, it was felt these added unnecessary complexity considering a separate 16 channel analog input card was already needed which provided 16 additional DIO lines. Table 3.2 shows the usage of the G1 modules in the system.

Table 3.2: OPTO-22 Digital Signal Conditioning Modules

Module Description	Module Model	Signals
Reed / mechanical relay for DC (replacing the Versalogic pn 2312 card)	ODC5R	Laser Key Switch Radar Button 1 Radar Button 2
5 to 60VDC output SSR *replaces the Power Relay Driver card outputs	ODC5	Laser Shutter* Field Stop* Deck Power 1* Deck Power 2* Laser Power* Radar Enable* Audible Alarm* Open Hatch Close Hatch
5 VDC Input Module	IDC5D	Hatch Open Hatch Closed
90-140 VAC input module	IAC5	Deck Power Proximity Sensor 1 Proximity Sensor 2

It should be noted that the modules as shown in Figure 3.1 are arranged in what may at first appear to be an extremely counterintuitive pattern in that the two racks are divided between inputs and outputs; however, there is a reason that this arrangement was chosen. Since in the system the two PB16H racks will be stacked, it is less convenient to access the lower rack to insert or remove modules. To allow addition of new modules as either inputs or outputs, most "open" module slots are left on the top rack and modules which are not expected to be changed are put on the bottom rack.

Each rack is then divided between input and output bits to allow both open inputs and outputs to be readily available on the upper rack.

3.4.3 RS-232 Serial Ports

While the somewhat less reliable RS-232 link has been abandoned for the main console to deck computer communications, many devices in the deck unit still require it. The ones which are carrying over from the existing computer are the Oriel fiber positioner and the CU601 laser controller, the specifics of which can be found in their respective manuals. A third serial link is required in the new system to allow communications between the small STD bus computer and the main deck SBC; however, this can be eliminated on completion of the new radar and timing card discussed in Appendix B. Since the VSBC-7 provides four on-board serial ports there is no need for any additional hardware.

3.5 Reserved Resources

Since this system is being designed with an upgrade path towards ALAPS in mind, it seems clear that certain resources must be reserved in advanced. In many cases this should not be a problem as more than adequate resources have been left over for new additions. The first of these is a space on the PC104 stack which must be reserved for possible usage with a counting card as later described in Chapter 5. The PC104 specifications state that there should be no more than three PC104 cards stacked onto the computer card thus leaving two more cards allowed which seems adequate at the present time. The next set of reserved resources is for the P-Count unit from Marina Photonics. In preliminary discussions, the interface has been stated as most likely being

an RS-232 and Ethernet combination. While the reasoning for this is still unclear, both are provided for so long as a small Ethernet hub can be placed in the system when needed.

Chapter 4: Implementation Details

One of the largest problems in determining the details of the original deck computer was the lack of functional documentation. While schematics were present, there was little documentation which described the functionality and limitations of the circuit which necessitated some reverse engineering. In addition, when the functional documentation was present, there was rarely a source which could describe the reasoning behind the design decisions and provide indications as to the intended future uses or expandability of the system. Therefore, in this section the physical implementation will be described in detail as well as the reasoning behind a number of the less obvious physical design and wiring choices made.

As discussed in Chapter 3, the major components of this new system are the SBC, the PB16H digital modules, the 5B analog signal conditioning rack, and the 4-slot STD bus back-plane. In addition, an ATX main power supply is used for the SBC and STD computer power with an auxiliary power supply for the +12VDC and –12VDC. A small 24VDC breakout box is also used to distribute the 24VDC from the connector to the various modules on the PB16H racks. It is believed that the design decisions described in this chapter represent a balance meeting the primary goals of using off-the-shelf hardware, providing flexibility, and minimizing risk of breaking existing critical systems.

4.1 Physical Design and Wiring

A top block-level view showing the major components' rough locations in the re-designed system is shown in Figure 4.1. While a detailed mechanical drawing of the chassis was used during initial fabrication, it was heavily modified by hand after being

machined. Therefore, a new mechanical drawing should be created if needed in the future.

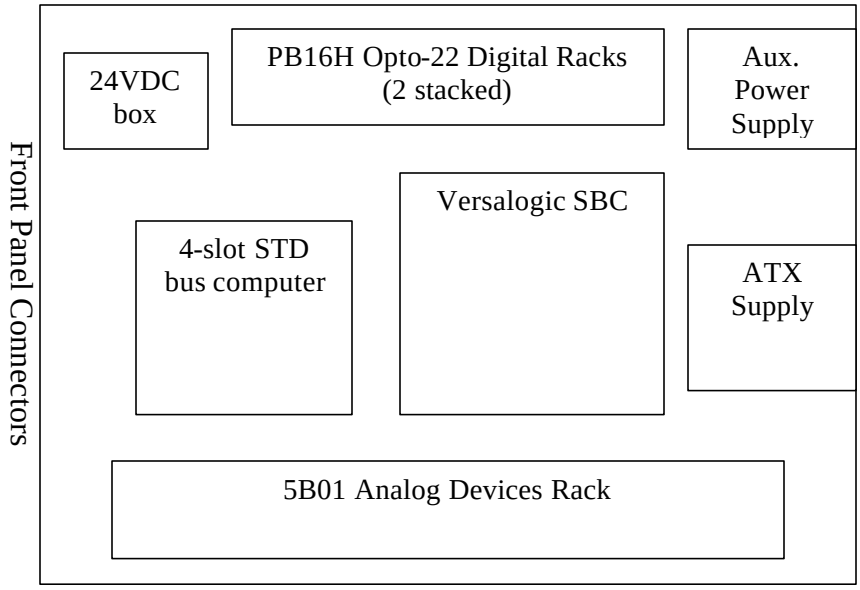
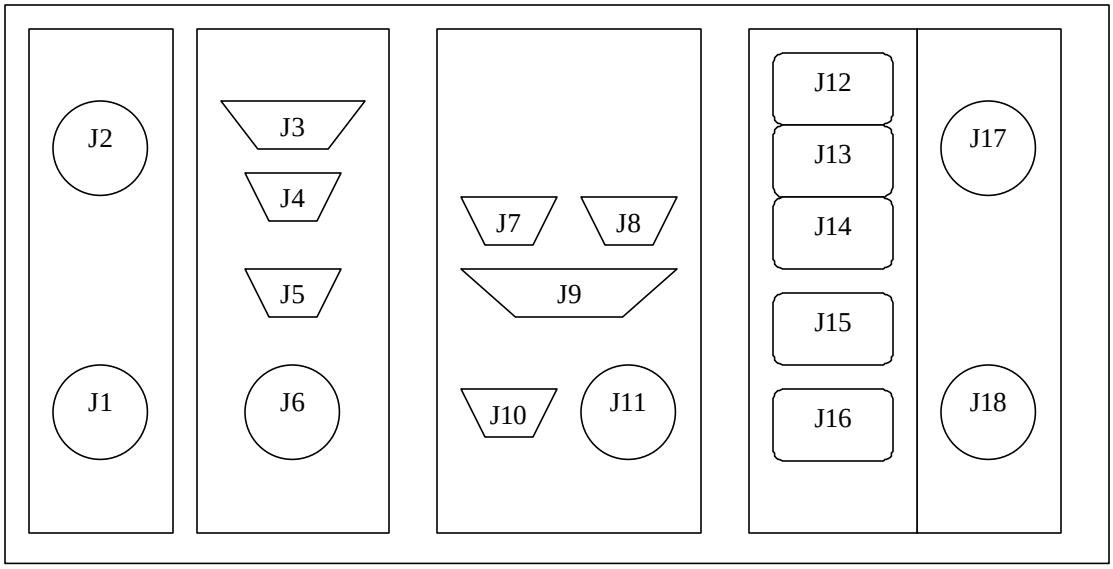


Figure 4.1: Block Location Diagram for New Computer (Top View)

In the early stages of the physical design of the system, it was determined that it would be beneficial to reuse many of the connectors that were already on the existing computer. For this reason, the existing face from the STD bus computer was simply removed from the rack mount STD bus chassis and mounted to the shell in which the new computer would reside. This allowed the modular panels from the existing computer to be reused where desired. In other cases, the cables could be rewired and the panels modified accordingly. The redesigned front panel is shown in Figure 4.2 which may be compared to the old faceplate in Figure 2.5.



* Figure not to scale

Figure 4.2: Layout of New Deck Computer Faceplates

As can be seen from Figures 4.1 and 4.2, the front panels are laid out in such a way that they provide a fair indication of where the signals are routed and provide a clear routing path to their destinations in most cases. Also, all of the panel connectors from the radar and timing cards were reused and connected to their STD bus cards as in the original computer. The connectors for the digital signals have been changed over to circular plastic connectors (CPCs) primarily due to cost concerns; however, MIL-SPEC connectors could be used to replace the CPCs if necessary. Also, the panel which previously had contained the four thermocouple inputs now contains two of the original thermocouple jacks and three RTD jacks. The intent had been to replace all thermocouples with RTDs; however, appropriate probes for the chiller hose and DI water reservoir could not be found so the originals were kept in place and reused.

Cooling for the system is provided by the three exhaust fans which were present at the top of the rack. One problem, which was not anticipated in the physical design, is the fact that the solid sheet metal construction of the rack mount shell does not provide a large amount of cooling for the radar control electronics which sit in the next rack slot below. This has not caused a problem so far, but any re-design should address this issue by providing vents in the bottom of the chassis.

Table 4.1: New Deck Computer Faceplate Connector Descriptions

Connector	Description	Old (Figure 2.4) Connector Label If Carried Over
J1*	DIO 1 (see Table 4.2)	-
J2*	DIO 2 (see Table 4.3)	-
J3	Open DB-25 mount	-
J4	DB-25 for mechanical relays to radar system (see table 2.6)	J12
J5	DB-9 signals from radar system to radar card (see Scott Boone thesis)	J13
J6*	Timing card output to console and CU601 externals (see Table 2.5)	J6
J7	COM 3 (CU601 Link) J-Type thermocouple connector for deck temperature 1	J11
J8	COM 4 (Fiber motor controller) J-Type thermocouple connector for deck temperature 2	-
J9	Open DB-25 mount	-
J10	Monitor output for STD bus computer	J4
J11	AT-style keyboard connector for STD bus computer	J5
J12	RTD input for AC temp	-
J13	RTD input for deck temp 1	J7 **
J14	RTD input for deck temp 2	J8 **
J15	J-Type thermocouple input for chiller water temperature	J10
J16	J-Type thermocouple input for laser DI water temperature	J9
J17	Analog input from terminal strip (see Table 2.8)	J15
J18	Analog input from laser (energy monitors). power for energy monitors and connection to relay driver card for laser shutter (see Table 2.9)	J16
* Pin descriptions given in separate table ** Connection not identical to old computer, but functionally or logically similar		

The wiring for the majority of the system is fairly straightforward and simple which was a goal of the re-design along with using only COTS parts. The method of using screw terminal signal conditioning racks which interface to the SBC over ribbon cables provides for a straightforward and customizable wiring methodology, but

obviously requires more space. For this reason virtually all the schematics given will be in block diagram form rather than a formal schematic drawing. There are, however, a few cases where a decision was forced between making drastic modifications to external wiring and adding complexity to the internal system. One of these cases involved the OPTO-22 modules used to replace the Power Relay Driver card. The existing system used a setup roughly equivalent to that shown in Figure 4.3.

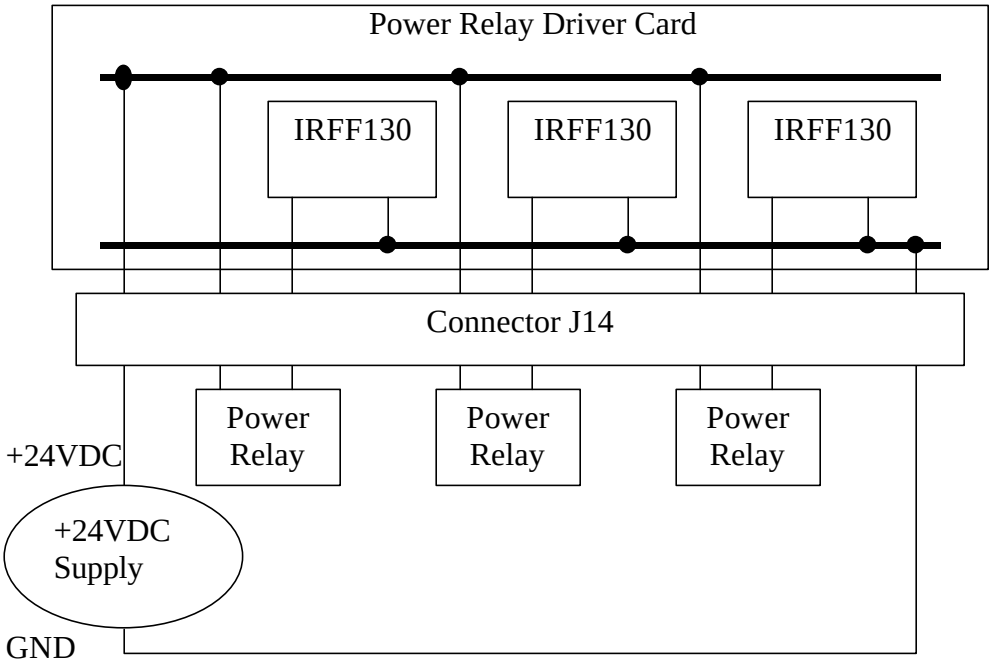


Figure 4.3: Old Deck Computer Power Relay Driver Schematic

While at first glance, it seemed odd to bring the 24VDC onto the STD bus card then back out to the power relays and then back into the SBC card, it is possible this may have been done as a safety. In such a design, +24V cannot be applied to the power relays unless the card is connected. While this still seems unusual, the new design uses a breakout box for the +24V to avoid a drastic rewiring of the system electronics, much of which has questionable documentation. The schematic shown in Figure 4.4 indicates

the method used in the new system. This schematic is also used for devices driven directly by the 24V supply such as the field stop solenoid.

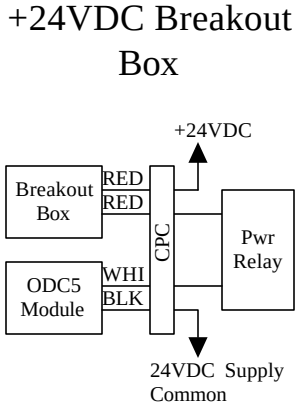


Figure 4.4: New Deck Computer Power Relay Driver Schematic

Overall, a standardized approach for wiring new connectors to IO module racks has been used wherever possible. The method used simply wires from pin N to terminal N on the module rack. Note that some of the modules are used to drive items which were left connected to the original connectors, the kill switch for example. In this case wiring from the PB16H terminal strips are not routed to J1 or J2 but to J6, the reused connector from the old computer faceplate. Therefore not all modules are wired to the corresponding pins on J1 and J2, but those that are, have been connected as described above when possible. The detailed pin-outs for J1 and J2 of the new computer are given in Tables 4.2 and 4.3 respectively.

Table 4.2: New Computer Faceplate J1 Pinout

Pin #	Description	Internal connection(s)*	Pos. On orig. Faceplate (if present)
1-6	not connected		
7	Proximity Sensor 2+	PB16H(b), 7, IAC5+	J17-A
8	Proximity Sensor 2-	PB16H(b), 8, IAC5-	J17-B
9	Proximity Sensor 1+	PB16H(b), 9, IAC5+	J17-C
10	Proximity Sensor 1-	PB16H(b), 10, IAC5-	J17-D
11	Deck Power Sensor +	PB16H(b), 11, IAC5+	J17-E
12	Deck Power Sensor -	PB16H(b), 12, IAC5-	J17-F
13-16	not connected		
17	Deck Power 2 Control	PB16H(b), 17, ODC5+ ***	J14-N
18	24VDC For Deck Power 2	24VDC breakout box	J14-P
19	Deck Power 1 Control	PB16H(b), 19, ODC5+ ***	J14-R
20	24VDC For Deck Power 1	24VDC breakout box	J14-S
21	Laser Power Control	PB16H(b), 21, ODC5+ ***	J18-25
22	24VDC For Laser Power	24VDC breakout box	J18-13
23	Field Stop Control	PB16H(b), 23, ODC5+ ***	J16-D
24	24VDC For Field Stop	24VDC breakout box	J16-R
25	Audible Alarm Control	PB16H(b), 25, ODC5+ ***	J14-L
26	24VDC For Audible Alarm	24VDC breakout box	J14-M
27	Key Switch Control +	PB16H(b), 27, ODC5R+	loose wire
28	Key Switch Control -	PB16H(b), 28, ODC5R+	loose wire
29	Laser Shutter Control +, Laser Shutter Sensor -	PB16H(b), 29, ODC5+, *** PB16H(b), 6, IDC5-	J16-U
30	24VDC For Shutter, Shutter Open Sensor	24VDC breakout box, PB16H(b), 5, IDC5-	J16-P
31	Radar Power Control	PB16H(b), 31, ODC5+ ***	J14-E
32	24VDC For Radar Power	24VDC breakout box	J14-F
33-35	not connected		
36	Common From 24VDC Power Supply	PB16H(b), 18, 28, 22, 24, 26, 30, 32 **	J14-B
37	24V source	24VDC breakout box	J14-A

* Notation used for PB16H racks indicates top(t) or bottom(b) rack, screw terminal number, module type and + or – side of module

** Wired daisy-chained from terminal to terminal on PB16H rack

*** Drives a power relay wired as in Figure 4.4 or other 24VDC device

Table 4.3: New Computer Faceplate J2 Pinout

Pin #	Description	Internal connection(s)*	Pos. On orig. Faceplate (if present)
1-12	not connected		
13	Hatch Closed Sensor +	PB16H(t), 13, IDC5D+	
14	Hatch Closed Sensor -	PB16H(t), 14, IDC5D-	
15	Hatch Opened Sensor +	PB16H(t), 15, IDC5D+	
16	Hatch Opened Sensor -	PB16H(t), 16, IDC5D-	
17-29	not connected		
30	Hatch Close Command +	PB16H(t), 30, ODC5+	
31	Hatch Close Command -	PB16H(t), 31, ODC5-	
32	Hatch Open Command +	PB16H(t), 32, ODC5+	
33	Hatch Open Command -	PB16H(t), 33, ODC5-	
34-37	not connected		
* Notation used for PB16H racks indicates top(t) or bottom(b) rack, screw terminal number, module type and + or – side of module			

The wiring for the Compumotor hatch can be understood more easily after reading the Compumotor controller manual which should be looked over before attempting any modifications[8]. All inputs and outputs are opto-isolated signals and there is a 5VDC power output available on the Compumotor controller to provide power to for these and the hatch sensors. The controller has four opto-isolated inputs which are used, “I1”, “I2”, “CW”, and “CCW” and it has been programmed such that I1 going active will signal the hatch to close, while I2 will signal the hatch to open. The CW and CCW limit inputs correspond to the hatch being open and closed respectively. This limit sensing is done by two hall effect sensors (Parker Automation pn. SMH-1N) on the hatch arm which take a 5-24VDC supply input on two leads (brown and blue) and drive a load at this voltage on the third lead (black)[17]. This sensor output is received by both the Compumotor controller and the OPTO-22 module as in Figure 4.5. While the details are explained in the hatch controller manual, the basic operation can

be understood as follows. The power for all communications as well as the sensors comes from the controller's 5V output. The Opto1 and Opto2 lines on the controller are the input diode cathode for the opto-isolated inputs. For the CCW, CW, and IDC5D sensors, when the SMH-1N sensor becomes active, it allows a path through the sensor for current to activate the inputs as shown in the Figure 4.5, below. Note in the figure that if the "closed" sensor is not activated, there will be no current path to ground. For the ODC5 modules, the module provides the path to ground through the I1 and I2 inputs when activated. The inputs and outputs for the Compumotor control are on the J2 faceplate connector. In the original deck computer, these inputs and outputs were driven using TTL level buffers which is not appropriate for these sensors. This is because normal digital TTL lines typically drive inputs in the kilo-ohm range while the resistance of the opto-isolator input is in the hundreds of ohms. This new arrangement provides much better noise isolation as well as protection It should be noted that IDC5D modules are used for this circuit which is necessary because the IDC5 modules have a higher activation voltage which occasionally causes erratic behavior.

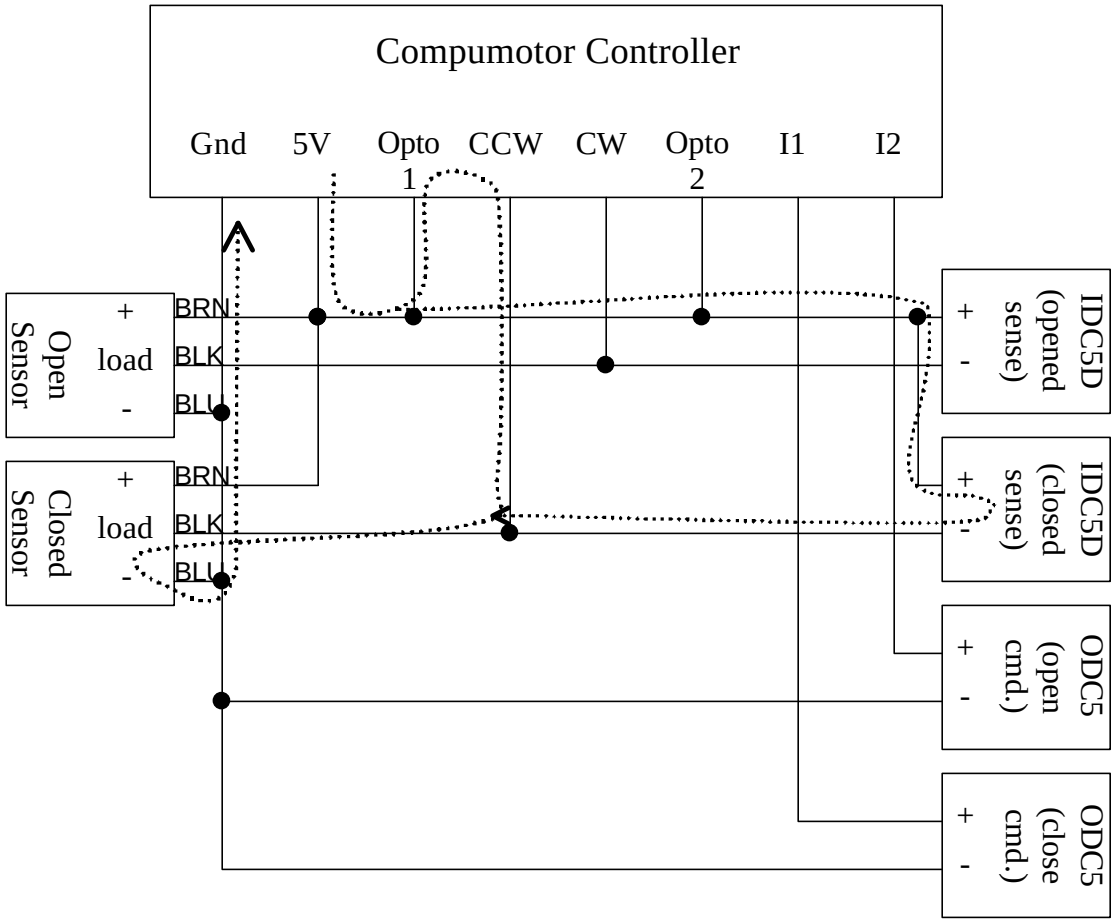


Figure 4.5: Compumotor Connection Schematic With Example Sensor Current Flow

The wiring for the temperature sensors has also been done in a relatively straightforward manner using standard connectors, as in the original system. Two of the four original thermocouple sensors were used for chiller and DI water temperature while the two old sensor points for deck temperature and the one new point for air conditioner temperature have been implemented using 3-wire RTD sensors. Both the sensors used and the panel mounts were obtained from Omega Engineering and are specified in Table 4.5.

The wiring of the J6 connector for the CU601 externals and the CAMAC timing signals is nearly identical to the original deck computer, with the exception that the kill switch status is now read via an OPTO-22 IDC5 module. An interesting troubleshooting point should also be noted regarding the 5VDC provided across pins 54 and 55 of this connector. If this 5VDC signal is not present, the laser will flash once and then enter its "simmer" state rather than continuing to flash. While the reason for this is not clearly understood it seems that a constant high signal on this line is sufficient to cause the capacitor banks in the laser electronics rack to charge without needing a signal edge sometime relative to the "fire" signal. Leaving this line low causes the capacitor banks to not recharge after firing

4.2 Power Consumption

While given our use of a 300 watt ATX power supply power should be plentiful, an estimate of the current on each output leg of the main power supply will be given here in case more features are added which will draw a large amount of current. It should be noted that a large number of these current figures are estimates, typically far over what is likely. There are also a number of small components which draw minor amounts of current such as those that drive opto-isolators and such.

Table 4.4: Current Consumption for Deck Compter Devices

Device and Reference if Avalible	Current Drawn From Source				
	ATX 5V	ATX 12V	Aux. –12V	Aux. +5V	Aux. +12V
VSBC-7 [19]	5.80A	0.00A	-	-	-
DAS-1 [20]	0.51A	0.02A	-	-	-
5B32 modules (2) [3]	0.06A	0.00A	-	-	-
5B34 modules (2) [3]	0.06A	0.00A	-	-	-
5B37 modules (2) [3]	0.06A	0.00A	-	-	-
5B31 modules (4) [3]	0.12A	0.00A	-	-	-
STD Computer Card [21]	1.08A	0.00A	-	-	-
Radar Card (est.)	2.00A	0.00A	-	-	-
Timing Card (est)	2.00A	0.00A	-	-	-
Energy Monitors (est.)	-	-	0.25A	-	0.25A
TOTAL	**11.69 A**	**0.02A**	**0.25 A**	**-**	**0.25 A**

4.3 Parts List and Cost Goals

As one of the goals for the project was costing less than $6,000 for all hardware, the amount spent will be discussed here. Also given is a list of parts which may need to be replaced in the future due to breakage or expansion of the system. Table 4.5 does not list all parts ordered as some parts were tried and deemed inappropriate, or were not used due to changes in the overall design. These “unnecessary” parts along with those ordered as field spares contributed approximately $350 to an overall total of approximately $4750.

Table 4.5: List of Major Parts For Upgraded Deck Computer

Description	Category	Source	Part #	Unit Cost	# Needed
5B module 4-20mA in 0-5V out	analog sig cond	Analog Devices	5B32-01	$ 112.50	2
5B module 100ohm RTD, 0-100C	analog sig cond	Analog Devices	5B34-02	$ 153.00	3
5B module -5 to 5V in 0-5V out	analog sig cond	Analog Devices	5B31-05	$ 112.50	1
5B module -5 to 5V in, -5 to 5V out	analog sig cond	Analog Devices	5B31-02	$ 112.50	3
5B module J-type thermocouple in	analog sig cond	Analog Devices	5B37-J-01	$ 112.50	2
5B01 16 module rack	analog sig cond	Analog Devices	5B01	$ 360.00	1
4-slot STD32 rack	computer	Versalogic	V32-04T	$ 194.00	1
DEV-007 Accessories for SBC	computer	Versalogic	DEV-007	$ 119.00	1
VCM-DAS-1	computer	Versalogic	VCM-DAS-1	$ 325.00	1
VSBC-7	computer	Versalogic	VSBC-7	$ 1,180.00	1
OPTO-22 G1 module iac5	digital sig cond	Newark	96F1013	$ 14.12	3
OPTO-22 G1 module idc5d	digital sig cond	Newark	96F1018	$ 12.89	2
OPTO-22 G1 module odc5	digital sig cond	Newark	96F1024	$ 14.40	9
OPTO-22 G1 module odc5r	digital sig cond	Newark	96F1026	$ 15.61	3
OPTO-22 G1 module PB16H rack	digital sig cond	Newark	92F3474	$ 80.56	2
7/8" #6 spacers for SSR racks	misc	Mc Master	92320A348	$ 1.28	6
Astec LPT42 power supply	misc	Newark	92F5315	$ 31.72	1
100' spool 2 cond, 20 ga	wiring	Newark	02F9063	$ 19.00	1
100' spool 4 cond, 20 ga	wiring	Newark	02F9069	$ 29.47	1
26pin sock to sock ribbon cable	wiring	Digikey	A3AAG-2618G-ND	$ 5.16	1
37 pin CPC plug	wiring	Newark	44F8392	$ 3.16	3
37 pin CPC socket	wiring	Newark	44F8393	$ 2.44	3
3-wire RTD Sensor	wiring	Omega	RTD-2-F3102-72-T-OTP-M	$ 58.75	3
RTD panel mount	wiring	Omega	TPJ-U-F	$ 4.50	3
50 pin sock/sock ribbon cable	wiring	Digikey	A3AAG-5018G-ND	$ 9.83	1
Connector for 92F5315 Astec power	wiring	Newark	93F9647	$ 0.43	1
Connector for 92F5315 Astec power	wiring	Newark	93F9659	$ 0.56	1
Pins for connectors for Astec power	wiring	Newark	93F9690	$ 0.08	12
CPC cable clamps large	wiring	Newark	87F1718	$ 4.63	8
CPC crimp pins (100pk)	wiring	Newark	96F7935	$ 31.20	1
CPC crimp sockets(100pk)	wiring	Newark	96F7936	$ 37.20	1

4.4 Known Faults

In the redesign of the computer system, a number of problems which were not particularly severe or did not impede operation of the system were discovered. Some of these have been mentioned previously and are repeated here for completeness. One of the largest problems with the system in its current form is its physical design. The material chosen for the computer rack chassis prototype was steel which is both prone to corrosion and extremely heavy. The weight of the system is a problem since the position in the rack is approximately six feet above the ground the system is resting on. In the field this would likely be even higher as the system is typically set on wooden boards for leveling purposes. A second problem is the previously mentioned cooling of the radar electronics mounted below. The solution to both of these problems is a complete will require a physical redesign of the chassis mount.

The recommended way to structure a redesigned system would be to use aluminum rather than steel due to its light weight and to design as an open frame rather than as an enclosed box. This would allow heat to easily rise from the electronics below. Most likely, an ideal design would turn the 5B and OPTO22 module racks on their sides so their screw terminals faced upwards. Cross supports in the center could be used to mount the SBC which should be mounted with flexible standoffs to prevent damage by flexing of the computer board as well as providing vibration protection.

Another physical design fault is that the re-use of the original computer's faceplates in different positions on the rack has created some open gaps. While this is largely an aesthetic concern, it is possible that objects could somehow enter these gaps shorting the nearby STD computer backplane cards. This problem can easily be

remedied by machining a new faceplate which fits more exactly the new system of connectors.

4.5 Installation of RT-Linux

The installation of the RT-Linux extensions is a fairly straightforward process and easily adaptable to new Linux kernels as they are released. However, as the installation instructions may change slightly from version to version, a general outline will be provided here along with pointers to where the most current information should reside. It is recommended that the newest versions of Linux and the RT-Linux extensions be installed when needed as they may provide bug fixes and improved performance. It is also recommended that anyone attempting any major modifications to the system be familiar with both the boot-up procedure for Linux and the working of the operating system. Nearly all needed reference information can be found at http://www.linuxdoc.org in the various HOW-TOs and guides.

The RT-Linux installation is started by performing an installation of a standard Linux distribution, in the case of this thesis, Redhat 7.0. The distribution may be installed with whatever options are desired as long as the following criteria are met:

- The Linux kernel compiler, kgcc, must be installed in order to compile the RT-Linux kernel modules. The standard gcc compiler must also be installed.
- Some telnet (or SSH) daemon should be installed in order to allow remote access to the deck system over the network.
- It is HIGHLY recommended that no X-Windows interfaces such as Gnome or KDE are installed as these are a waste of space in this system.

- Any SAMBA tools available should be installed to permit easier file access from the LAPS Console.
- Some editor, which works well over a telnet terminal, such as pico, should be installed for remote file editing.

Once the desired Linux distribution is in place, both the source code and instructions for installation can be obtained from Finite State Machine Labs Inc. (http://www.fsmlabs.com/), who currently distribute and support the RT-Linux operating system. This site will be able to provide detailed instructions on exact installation procedures which, in version 3.1 of RT-Linux, was located in "installation.txt" inside of the downloaded compressed file. A general overview to provide an idea of what is involved in the process will be provided here. The first step will typically be to download the source code for a specific Linux kernel. Next, the RT-Linux extensions patch to the standard kernel will be applied, and the kernel will be compiled. When compiling the kernel, be sure to enable any options such as SAMBA file system support or needed hardware drivers. Finally the new kernel is added to LILO such that it will boot. The LAPS software should then be copied to the new computer and re-compiled to ensure the executable is compatible with the installed kernel version.

Chapter 5: Conclusions and Future Directions

While the performance of the new deck computer structure remains to be tested in a full field campaign, the performance in the laboratory and during development has shown positive results. From finishing the UDP/IP communications link in October of 2001 to the current time, the communications link has proved extremely stable from both the RTLinux and Windows 2000 Console computer sides. In addition, there have been very few occasions on which the deck system has crashed which were not directly attributable to a programming or configuration mistake during development. The initial impression is that this should provide an extremely stable platform which can be expanded upon into ALAPS.

As the purpose of this thesis is to provide a starting point from which LAPS may begin its transition into a more ALAPS-type unit, some suggestions will be given here as to how to proceed. Since the redesign of the computing system has been done with some future methodology in mind, following this procedure should make the transitions as simple as possible with regards to their computer and control interfaces. Work not part of this thesis, but loosely related, has also been taken into account in these recommendations. The main points to be addressed fall into three areas in which the LAPS system will be modified to meet its ALAPS goals, physical design issues, data acquisition issues, and optics issues. While each of these are related to each other in some aspects, some concurrent work may be done for many items.

The majority of the new features to be added to the LAPS unit require some physical and power wiring modifications to the deck unit. Two of these would be considered major tasks. The first task is the removal of the current window-type air

conditioner for cooling and use of a central air conditioner which supplies air to the system via a duct of some type. This transition helps to free space for approximately 12" of additional rack mount electronics below the existing laser electronics. As the US Navy specifications for ALAPS have specified that chilled air would be provided by the ship systems[10], this is feasible for the prototype. The second, and possibly most difficult, will be the rewiring of the LAPS unit to remove the breaker panel which is currently installed. This is necessary as it occupies the other half of the rack space where the air conditioner is located. The reason this rewiring may be difficult is that it is not known whether some of the wiring choices were made in order to meet requirements for a military prototype. In any case this must be done with great care and by someone who is very familiar with AC power wiring.

Two optics areas are also points of major work, and will require physical integration into the system. The first, and most important, of these two is the design of a more compact detector box. Given the reduced size of modern PMTs it is possible to easily reduce the entire detector box, including PMTs into a 19" rack mountable module which would be approximately 12" high for the proposed self-calibrating version and approximately 4" high for a non-calibrating version such as the current design. This design should be independent of the data acquisition system and the high speed PMT front ends expected from Marina Photonics. The second major area for optical design work is the implementation of a folded telescope design. This design would free a large amount of space, roughly 10%-15% of the current volume of the system assuming the telescope is folded to half the height of the current LAPS telescope and the telescope currently occupies roughly 25% of the LAPS volume.

The data acquisition systems and PMTs capable of operating at a count rate of over 700MHz are well underway in design; however, it is the belief of the author that waiting for these systems to be finished before designing the new detector system would be unnecessary. The most suitable way to proceed is by developing and testing a new detector box using current commercially available PMTs which count at a rate comparable to the currently used devices, about 100MHz. As these occupy roughly the same space as the anticipated high speed counters a later upgrade would be trivial. It is also understood that commercially available PC-104 format cards exist for counting at rates equivalent to the current system. This would allow the elimination of virtually all of the Console unit and extensive testing of the new detector box before transitioning to the new detector and counting system. If either the AC unit and breaker panel are removed from the deck unit or the folded telescope design is implemented, than room will exist for the new detector box to move immediately to the deck system. If not, then the detector box and counting cards may be installed in the Console unit and Console computer for testing. The transition to a data acquisition system triggered off of a photodiode rather than a timing card would also be a task in this category; however, this cannot be implemented until using the next generation PCount systems.

In conclusion, it is hoped that this thesis will serve to provide a stable and expandable control electronics structure upon which these future improvements may rely. The system provides interfaces to control all anticipated new hardware improvements as well as the processing power to generate real-time data products while maintaining control over necessary safety systems. From all observations to this point, the new computer and electronics system seems to have solved many of the problems

observed in testing the original system while introducing relatively few additional difficulties.

List Of References

[1] Agilent Technologies, "High CMR, High Speed TTL Compatible Optocouplers", 1999, http://www.semiconductor.agilent.com

[2] Agilent Technologies, "AC/DC to Logic Interface Optocouplers", 1999, http://www.semiconductor.agilent.com

[3] Analog Devices Inc., "Analog Devices 5B Series User's Manual", Analog Devices Inc. Norwood, Massachusetts, 1987

[4] Boone, Scott P., "A Digitally Controlled Safety Radar Subsystem for Atmospheric Lidar Systems", MS Thesis, The Pennsylvania State University, 1995

[5] Burr-Brown Corp., "INA102 Abridged Data Sheet", Document Reference "PDS-837E", 1985, http://www.ti.com*

[6] Burr-Brown Corp., "RCV420 Precision 4mA to 20mA Current Loop Reciever", Document Reference "PDS-523G", 1997, http://www.ti.com

[7] Chadda, Ginni

[8] Compumotor, "SX/SXF Indexer/Drive Users Guide", Compumotor Division of Parker Hanniflin Corp., 1993

[9] Continuum, "Operation and Maintenance Manual for the Powerlite 9000 Series Laser", Continuum, Santa Clara, CA, 1993

[10] C. R. Philbrick and D. B. Lysak, Jr., "Lidar Measurments of Meterorological Properties and Profiles of RF Refractivity", Proceedings of the 1996 Battlespace Atmospherics Conference, Technical Document 2938 NCCOSC RDT&E, pg 595-609, 1996

[11] DSP Technology Inc., "DSP Model 2090S Multi-Channel Scaling Module Reference Manual", DSP Technology Inc., Fremont CA, Jan. 1988

[12] DSP Technology Inc., "DSP Technology Model 4101 Reference Manual", DSP Technology Inc., Fremont CA, Oct. 1990

[13] Dallas Semiconductor, "DS1020 Programmable 8-Bit Silicon Delay Line", 1999 http://www.maxim-ic.com

[14] Intersil Corp., "IRRF130 Data Sheet", March 1999, http://www.intersil.com

[15] Marina Photonics, "P-Count I manual", Marina Photonics, Marina, CA, 1999

[16] Oriel Instruments, "Encoder Mike Controller, Model 18011", Oriel Instruments, Stratford CT, Jan. 1991

* Note that Burr-Brown Corp. has merged with Texas Instruments, hence documentation may be found on the Texas Instruments web site. Searching by Document Reference number works best.

[17] Parker Automation, “ET Series Stepper and Servo Driven Linear Actuators, Maintenance Instructions and Parts List”, Parker Automation, Wadsworth Ohio, Jan. 1998

[18] Finite State Machines, “RTLinux FAQ”, http://www.rtlinux.com, May 2001

[19] Versalogic, “VSBC-7 Reference Manual, Rev. 3”, Versalogic Corp., 2001, http://www.versalogic.com

[20] Versalogic, “VCM-DAS-1 Reference Manual”, Versalogic Corp., May 2001, http://www.versalogic.com

[21] Ziatech, “ZT 8902 Single Board Computer”, Ziatech Corp., San Luis Obispo CA, June 1993

Appendix A: New Deck Computer Code

Appendix B: Design Suggestions For Replacing STD Timing and Radar Cards

As referenced often in the body of this thesis, one of two steps should be taken relatively quickly in the progression of the LAPS system. Either the system should more towards exclusive use of the 3rd harmonic eliminating the need for a radar safety system, or a new radar and timing card should be designed eliminating the need for the solution involving the small STD bus computer currently used. As is seems, ozone-related research will continue so the latter is the more likely alternative. While working on this thesis, there was not sufficient time to design and test such a card, but much though had been given to the idea. The most straightforward methodology for designing a replacement for the small STD bus system would be a simple PCB containing two to three Complex Programmable Logic Devices (CPLDs). Part of the card should be as close as possible a copy of the radar card implemented by Scott Boone barring the STD bus interface. Close examination of his work reveals that the design features a mode where the system functions independent of the STD bus[4]. The other part of the card should be a refined version of the timing card design. One major change that should be made however is the addition of DIP switches on the card both for replacing the wire-wrapped adjustments and for setting the fine delays currently adjustable via software. Using these approaches, a card could be designed which would not need to interface to the computer via a bus, but could simply use the available parallel port of the computer to receive the necessary timing command bits and the radar commands. An input module on the PH16H rack already is designed to detect a bit indicating a radar detection. In addition the card could be designed so that the circuit simply disables the Q-switch signal in the event of a radar detection. The only

disadvantage of this scheme is the inability to receive an altitude for the target due to the lack of sufficient DIO lines to the SBC; however, if needed, a DAC could be used to output a voltage indicating range to one of the spare ADC channels on the SBC.

Given the existing design of the radar interface card and the simplicity of the timing functionality, this project would be of a level that can be easily accomplished either as an undergraduate senior design project or as part of a future master's level thesis encompassing increased functionality. A block diagram showing a basic layout of the considered design is shown in Figure B.1 below.

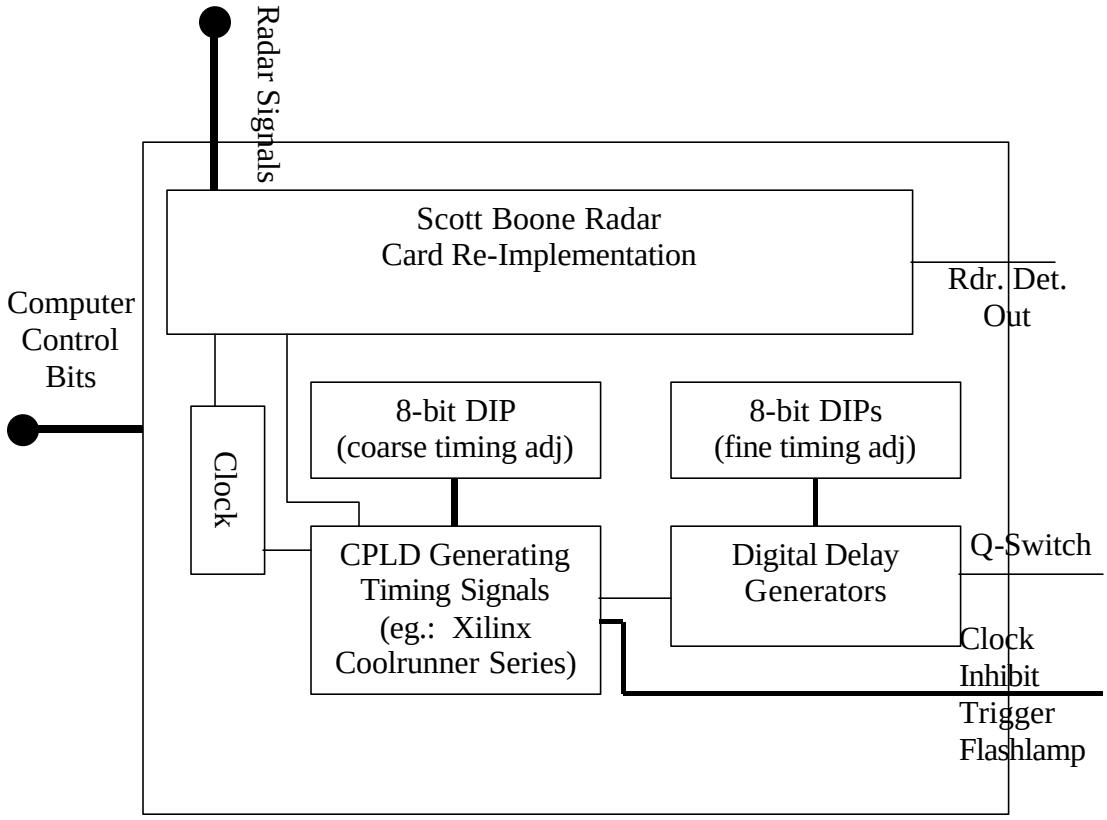


Figure B.1: Basic Design of New Timing and Radar Card

Appendix C: Overview of LapsConsole Software

In the original design of the LAPS system in 1995, a total of three computers were used; the computer in the deck unit and separate command and data display computers in the console unit. This was approach was because of the far slower computers available at the time the system was designed. Aside from requiring maintenance and upkeep of two aging computers and two separate programs in the console, the GPIB link between the two was a common source of problems. For this reason, over the Fall of 2000 and Spring of 2001 a single software package, LapsConsole v4.0, was written to replace the LapsDSP v3.x and LapsCommand packages. This program runs on a single computer and is designed in a highly modular fashion to facilitate system upgrades, for example the switch from a serial to Ethernet deck link. A second program called LapsProcessor is coupled with the LapsConsole software and is used for stand-alone post processing of the raw data; however, the LapsProcessor is not needed to acquire data. In fact the software is designed such that all processing and calculation modules are shared in compilation and the LapsProcessor can be thought of as a stripped-down LapsConsole with the ability to “acquire” raw data from the local hard disk rather than the CAMAC cards.

Due to the nature of this program’s use in a prototype, many possible optimizations or code shortening “tricks” have been avoided. This is because it is anticipated that future developers may not be entirely familiar with Windows programming or Visual C++ and working with the code should be as straightforward as possible. While as much as possible was left unchanged from the LAPS 3.x software, for various reasons almost all major portions of the software were rewritten.

One major change between the two software packages is the storage of raw data. In the LapsDSP software, data was stored both as an ASCII table and as a binary file. While this approach provides a small, quickly read binary file, it also means there are two data sets to archive, which is not deemed worth the effort given current computer speeds. Therefore it was decided to keep only the ASCII version as it is sometimes more portable, especially for Matlab and spreadsheet work. The LapsProcessor software is designed with the ability to read in LapsDSP v3.x data files and the format is very similar to the format used in the LapsConsole v4.0 files.

Another major change made to the architecture was changing from a standard PC tower to a rack mounted system from Cyber Research based on a Pentium-III computer card. This allowed freeing up of a large amount of space inside the console for use with new electronics. The only special hardware required in this new system is the CAMAC interface card which uses the ISA bus. A few features of this system should be noted. First, the computer card ordered contains an on-board sound card. The intended use of this feature was to install an outdoor speaker on the shipping container the LAPS unit Console is normally housed in for field campaigns. If the software is then modified to play sounds over the speakers (a simple task in Windows 2000), various alarms can be sounded in the case that an operator is not at the console.

The second feature of note on the card is the dual network adapters. This was done in order to allow the TCP/IP link to the deck computer to be on an entirely different subnet from the LAN which is normally connected in the shipping container during campaigns. If the deck computer were connected to the LAN along with the Console and other computers and a large amount of network traffic was created, this

could delay communications if the LAN is as in Fig C.1a. The setup in Figure C.2b avoids this problem.

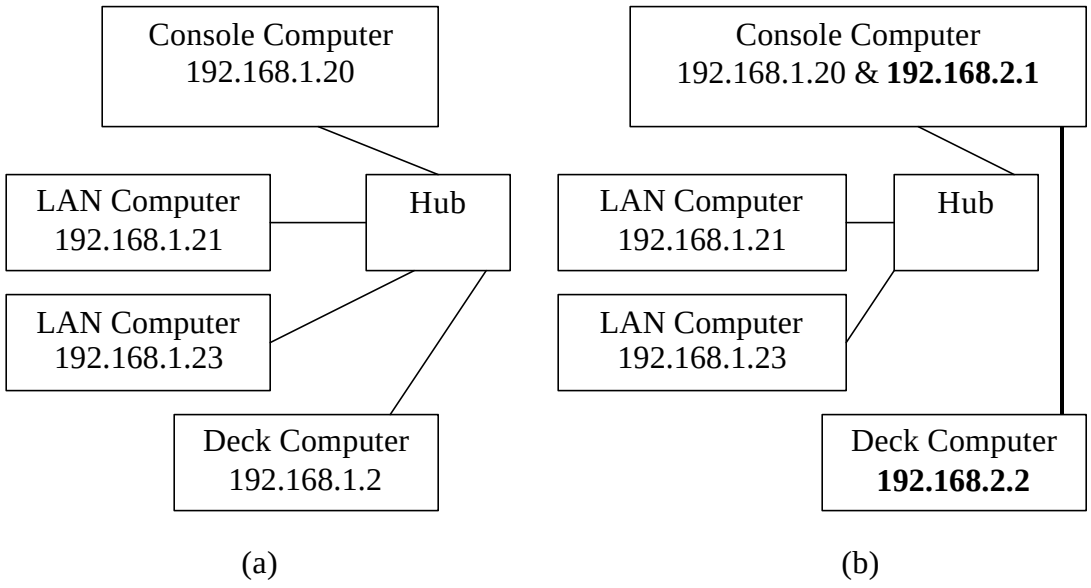


Figure C.1: Network Setup For New LAPS Console LAN

Appendix D: Matlab Code for DAQ Card and CAMAC Timing

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%% this file is to figure out the timings of the Q-Switch and CAMAC system
%%
%%  The timings needed are obtained as follows on a 400MHZ+ scope
%%    channel 1:  photodiode on top of hatch looking at beam
%%    channel 2:  clock signal from CAMAC unit
%%    ext trigger:   trigger signal on CAMAC panel
%%
%%    The delay can then be seen as below on the scope:
%%                    /-     -
%%    chan1    ------  \   / \   /-  /-V^V^V^v^v^--   a kind of ringing pulse
%%                      \_/   \_/  \-
%%    ----------------------------------------------------------------------
%%                   |---|   |---|   |---|   |---|
%%    chan2          |   |   |   |   |   |   |   |      500ns period clock(TTL)
%%             ----|   |---|   |---|   |---|   |---
%%
%%    the time from the first rising edge of the clock to the rising edge
%%    of the photodiode pulse is 'measuredBeamDelay'
%%    The rest of this program compensated for various delays in measument.
%%
%%    all units in meters and seconds

measuredBeamDelay = 620e-9;
CAMACBinUsedAsFirst  = 1;
metersPerFoot     = 2.54*12/100; % for conversions
c                 = 3e8;

fiberPropRate     = 0.7 * c;     % propagation rate of light in fiber
BNCCablePropRate  = 0.7 * c;     % rate of propagation of signal in BNC cable

%VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
% what delay is there from seeing light on chan1 to the expected photons
% hitting the CAMAC inputs oes through
% fiber->detector->PMT->Amplifier->Descriminator->CAMAC input
```

```
% fiber delays photon
fiberLength       = 75*metersPerFoot;        % length of reciever fiber
fiberDelay        = fiberLength / fiberPropRate;

% PMT travel time delays photon
PMTTravelTime     = 8e-9;

% cable from PMT to camac delays photon(assume 1m long)
PMTToCAMACAmpCableDel   = 1.0 / c;

% CAMAC electronics delay (these are just a guess for now
CAMACAmplifierDel       = 4e-9;
CAMACDescriminatorDelay = 1e-9;
CAMACInputToCountDelay  = 2e-9;

% how much delay did the photodiode cable introduce (assume 3 meters long)
PhotoDiodeCableLen      = 3.0;
PhotoDiodeCableDel      = PhotoDiodeCableLen / BNCCablePropRate;

% calculate total delay...this in essence shifts channel 1 to the right
TotalDelFromHatchToCAMAC = fiberDelay + PMTTravelTime + PMTToCAMACAmpCableDel...
   + CAMACAmplifierDel + CAMACDescriminatorDelay + CAMACInputToCountDelay;

% the cable from the photodiode to the scope artifically delays the pulse,
% so it was really earlier
TotalDelFromHatchToCAMAC = TotalDelFromHatchToCAMAC - PhotoDiodeCableDel;

% done, now we can compensate to say when the photons hit the CAMAC unit
%^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

%VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
% what delays are involved on the clock line

% cable delay from CAMACClock to scope
CAMACClkToScopeCableLen    = 10;
CAMACClkToScopeDelay       = CAMACClkToScopeCableLen / BNCCablePropRate;
```

```
% how long after the CAMAC gets a clock does it start a new bin(internal
%  electronics), a guess at this point
CAMACClkToBinDelay            = 2e-9;

% total delay compensation
TotalDelForClock              = CAMACClkToScopeDelay + CAMACClkToBinDelay;

% done
%^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

% shift chan1 to right by correct amount
compensatedBeamDelay = measuredBeamDelay + TotalDelFromHatchToCAMAC;

% shift chan2 to left
compensatedBeamDelay = compensatedBeamDelay + TotalDelForClock;

disp(['Compensated current delay from first clock edge to pulse is ' ...
      num2str(compensatedBeamDelay*10^9) ' nsec']);

%%%%
%% how much are we off altitude-wise
timeOffAfterBinShift    = (compensatedBeamDelay - CAMACBinUsedAsFirst*500e-9);
altOffAfterBinShift     = timeOffAfterBinShift * c / 2;

disp(['Taking into account CAMAC starting bin used, time off by ' ...
      num2str(timeOffAfterBinShift * 10^9) ' nsec']);
disp(['Taking into account CAMAC starting bin used, alt off by ' ...
      num2str(altOffAfterBinShift ) ' m (data shifted up)']);
```

Appendix E: Photographs of LAPS System

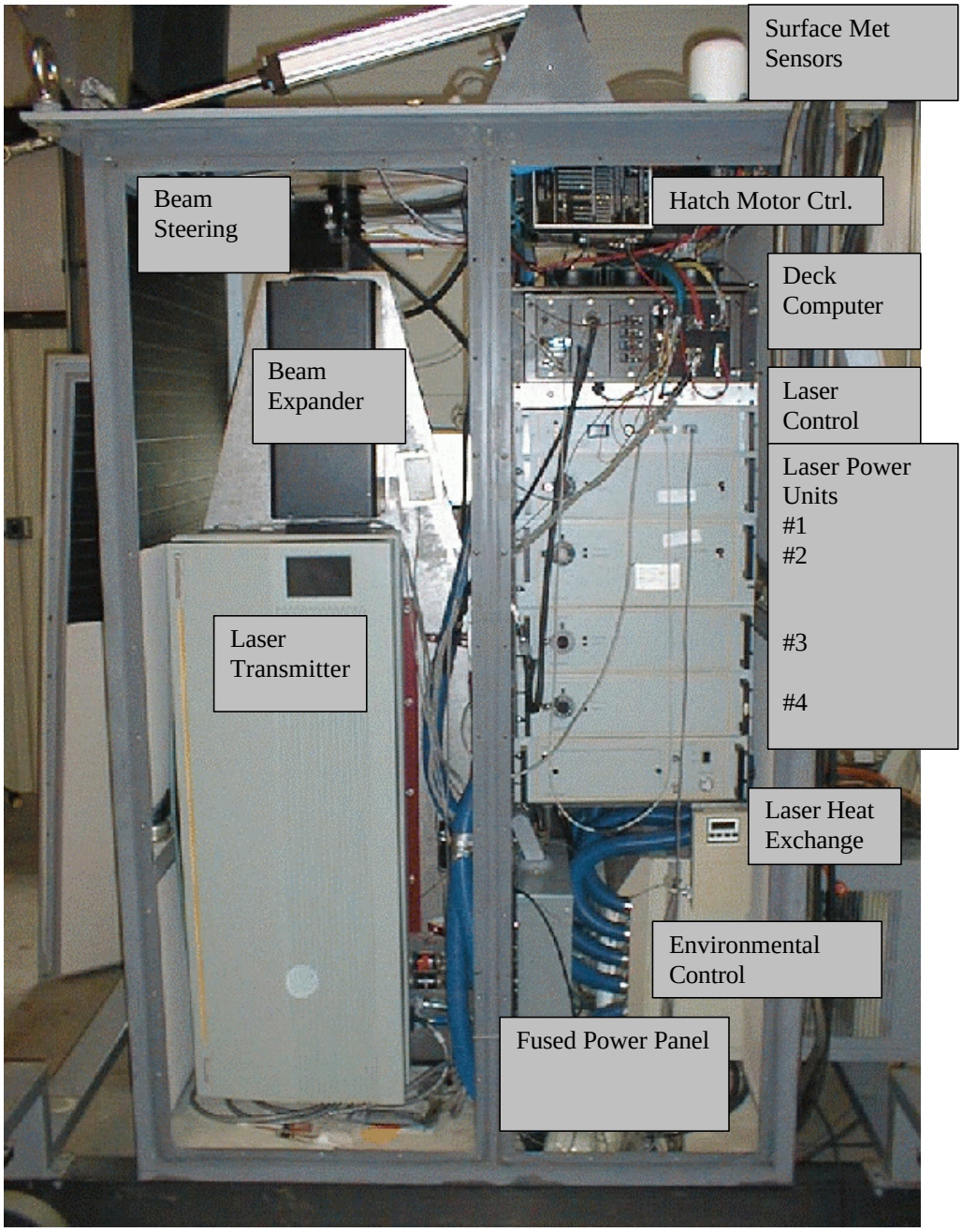


Figure E.1: Front View of LAPS Deck System

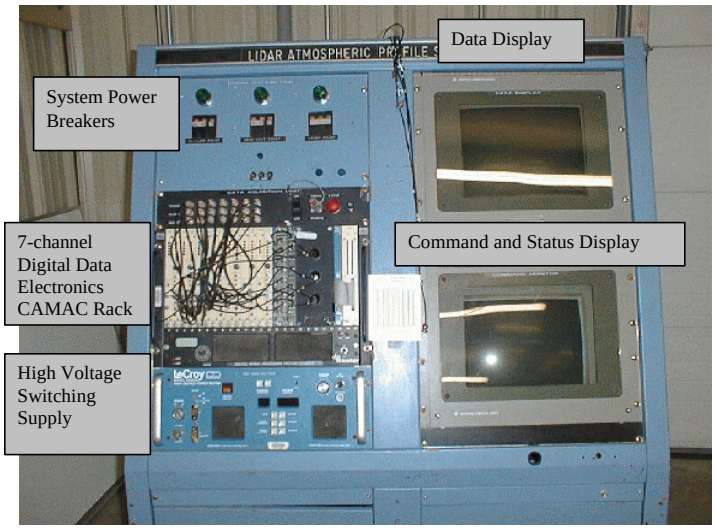


Figure E.2: Front View of LAPS Console (Spring 2001)

To Be Taken

Figure E.3: Top View of Redesigned LAPS Deck Computer

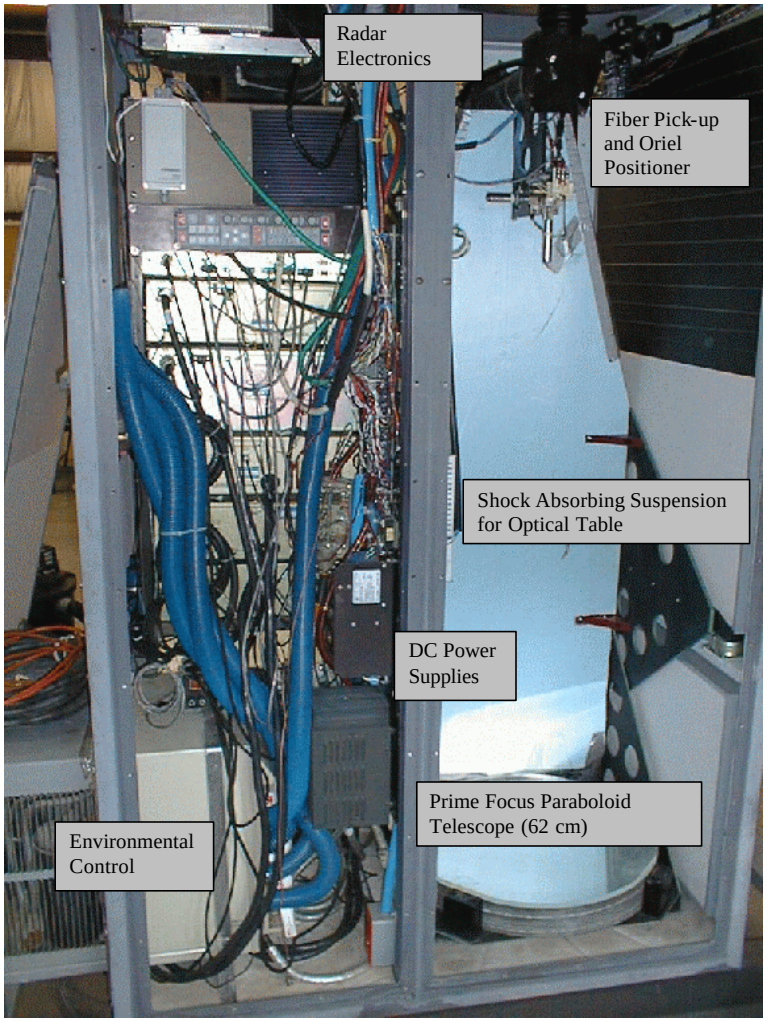


Figure E.4: Rear View of LAPS Deck Unit